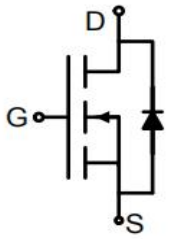
MXD30N50

N-Channel Enhancement Mode Power MOSFET

Description

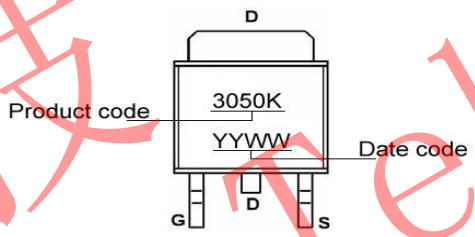
The MXD30N50 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$, with low gate charge .
It can be used in a wide variety of applications.



Schematic diagram

General Features

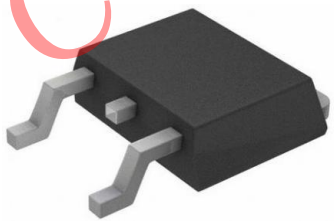
- V_{DS} =30V，I_D =50A
- $R_{DS(ON)}$(Typ.)7mΩ @ Vgs=10V
- $R_{DS(ON)}$(Typ.)11mΩ @ Vgs=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability



Marking and pin assignment

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-252-2L top view

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous(Tc=100℃)	I_D (100℃)	35	A
Pulsed Drain Current	I_{DM}	140	A
Maximum Power Dissipation	P_D	60	W
Derating factor		0.4	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	70	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

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Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30	33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.6	2	3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=25A	-	7	11	mΩ
		V_{GS}=5V, I_D=20A	-	11	16	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	15	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz	-	928	-	PF
Output Capacitance	C_{oss}		-	90	-	PF
Reverse Transfer Capacitance	C_{rss}		-	160	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V,I_D=20A V_{GS}=10V,R_{GEN}=1.8Ω	-	7.2	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	22.8	-	nS
Turn-Off Fall Time	t_f		-	8.1	-	nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=25A, V_{GS}=10V	-	14.3	-	nC
Gate-Source Charge	Q_{gs}		-	2.6	-	nC
Gate-Drain Charge	Q_{gd}		-	2.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=25A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	40	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs(Note3)	-	22	35	nS
Reverse Recovery Charge	Qrr		-	12	20	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω

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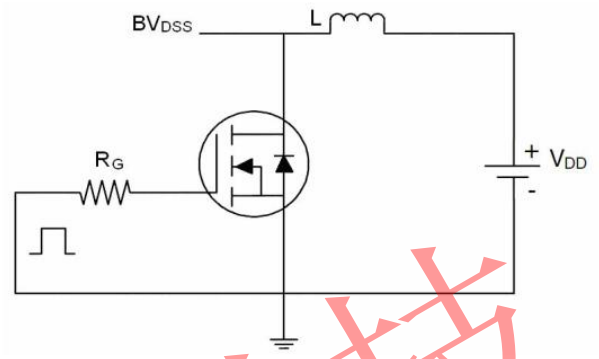
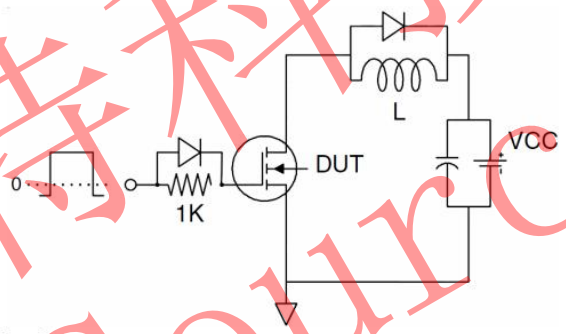
Typical Performance Characteristics

Test circuit

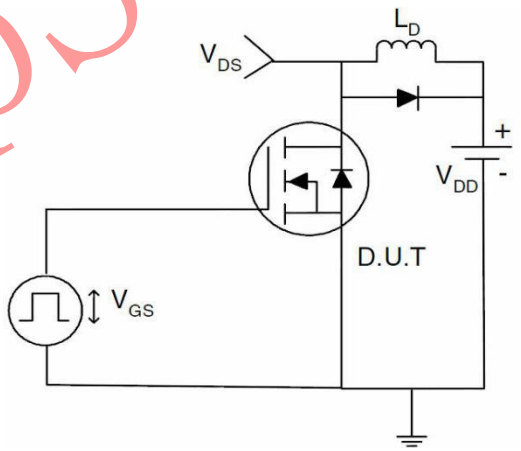
1）E_{AS} test Circuits



2）Gate charge test Circuit:



3）Switch Time Test Circuit:



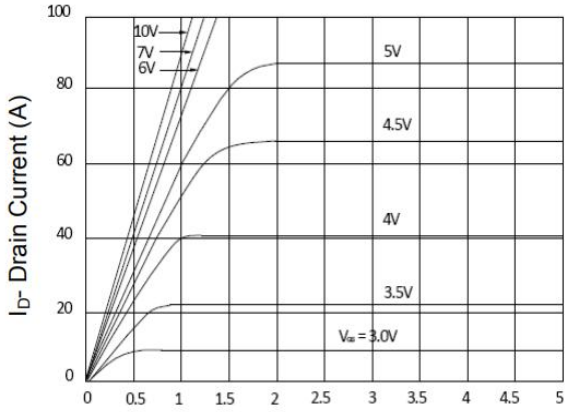
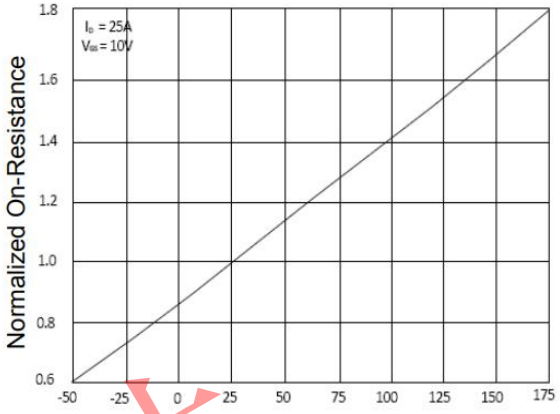


Figure 1 Output Characteristics Figure



4 Rdson-JunctionTemperature

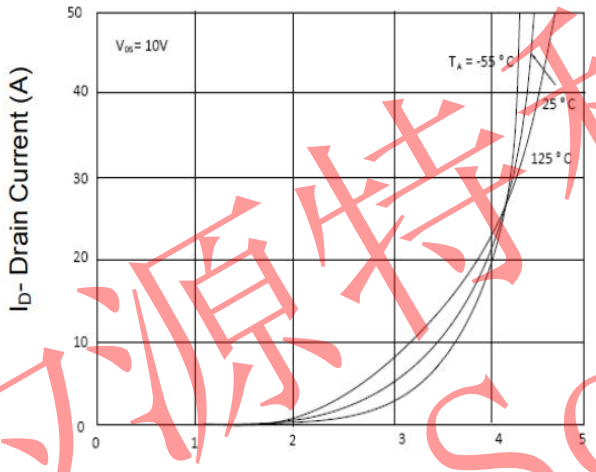


Figure 2 Transfer Characteristics

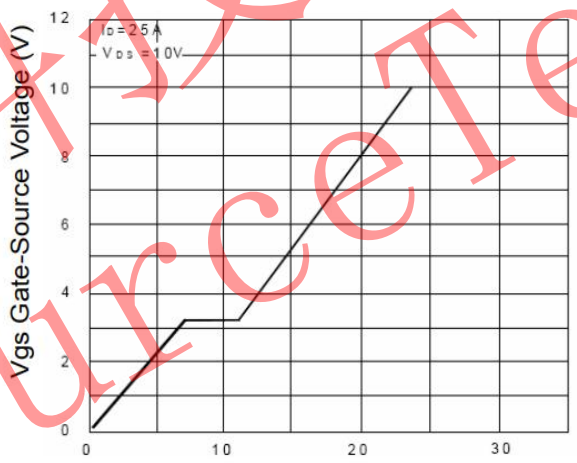


Figure 5 Gate Charge

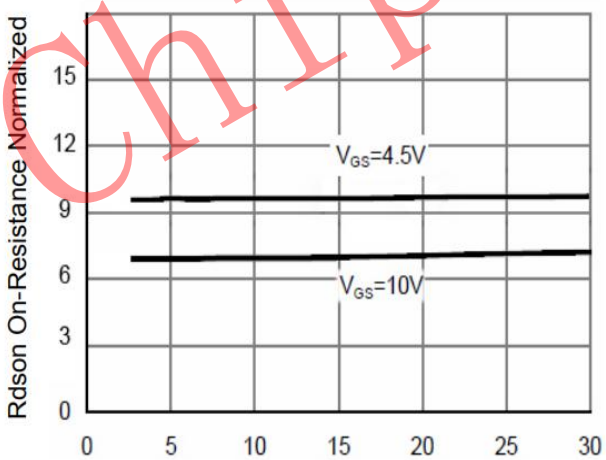


Figure 3 Rdson- Drain Current

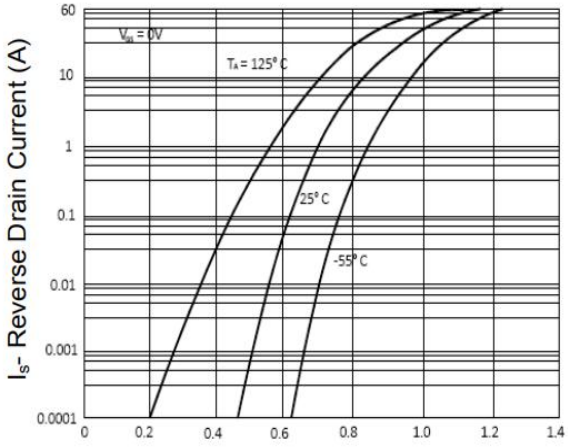


Figure 6 Source- Drain Diode Forward

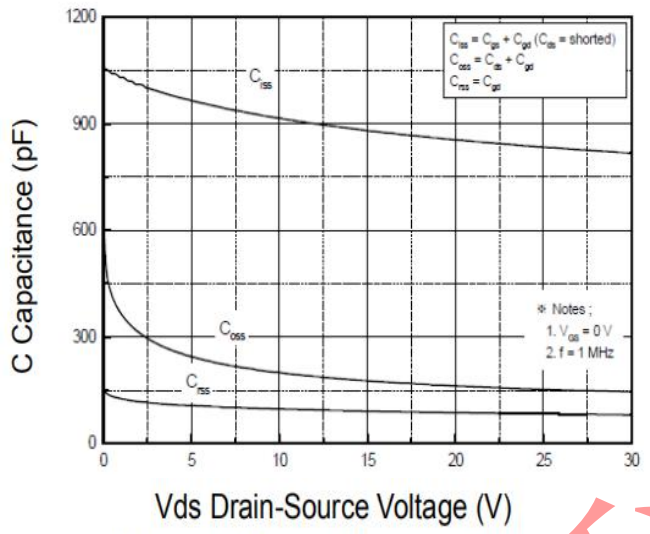


Figure 7 Capacitance vs Vds

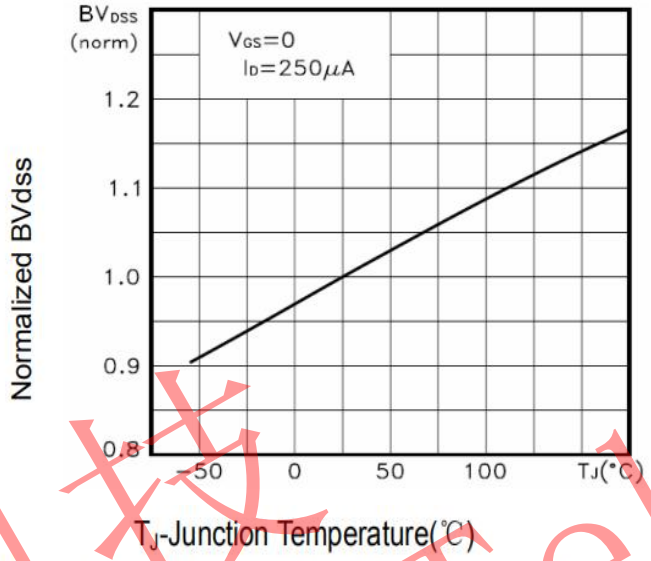


Figure 9 BV_{DSS} vs Junction Temperature

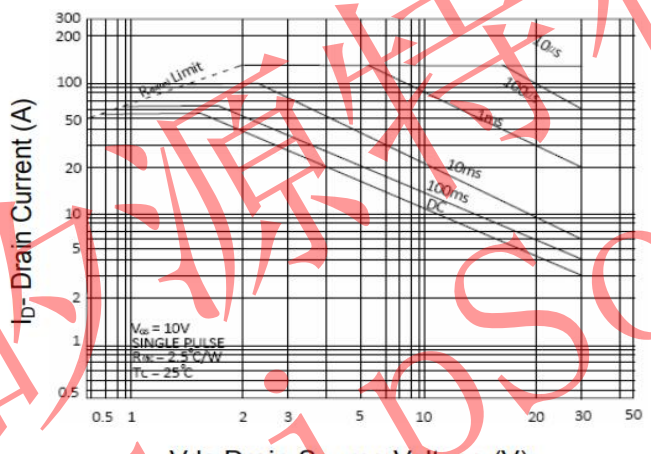


Figure 8 Safe Operation Area

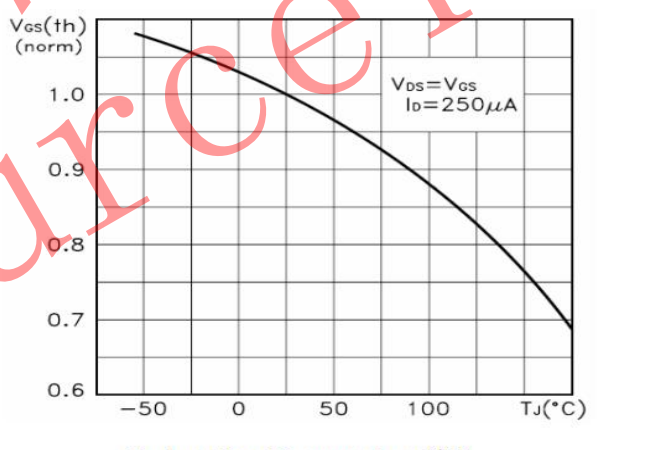


Figure 10 $V_{GS(th)}$ vs Junction Temperature

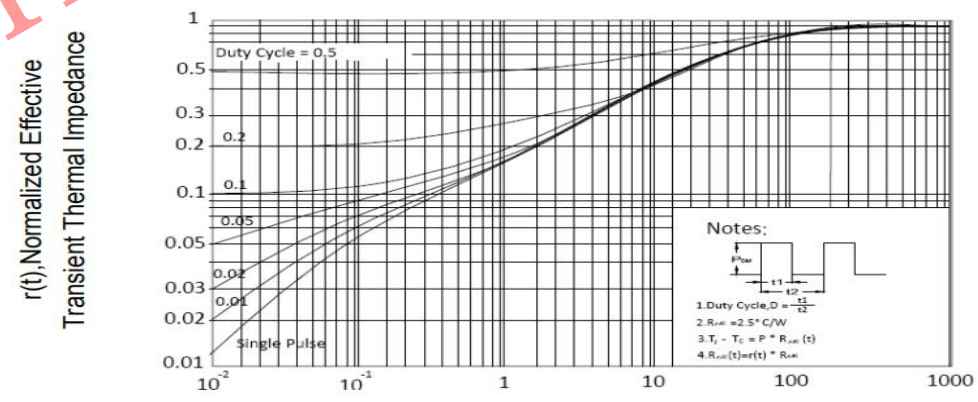
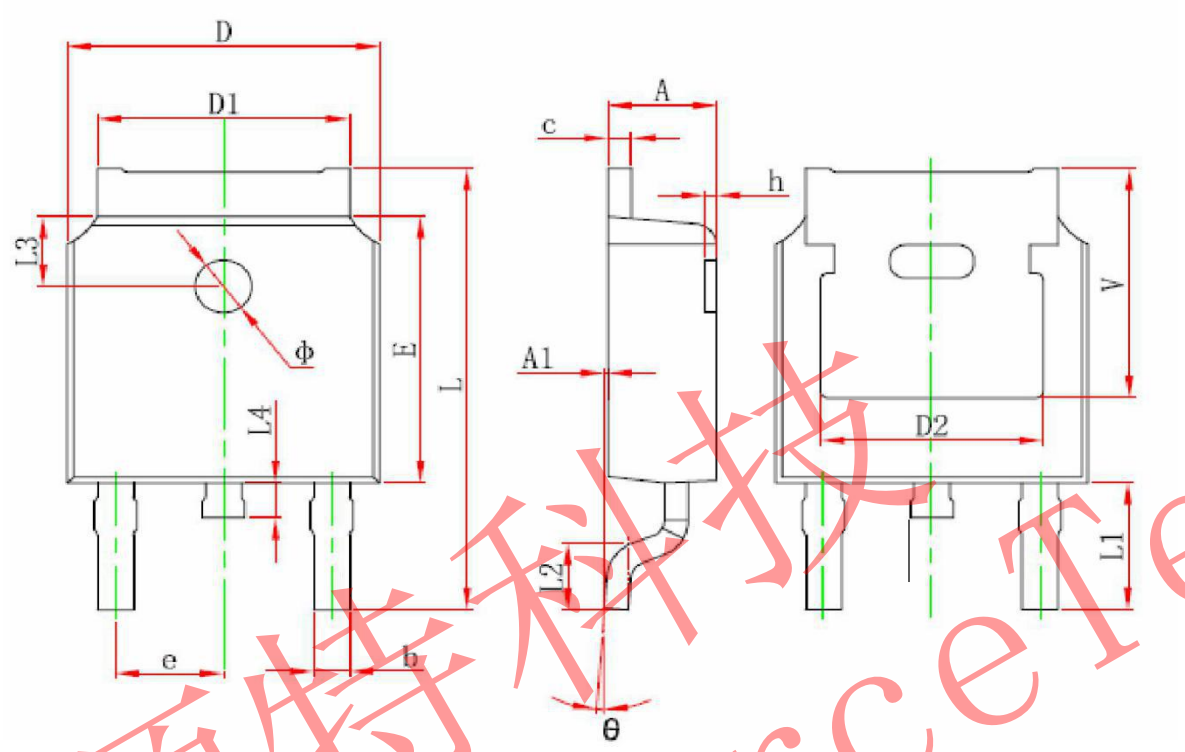


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	