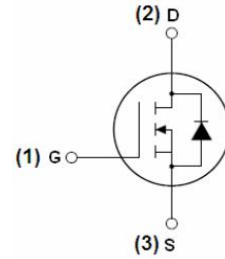




## N-Channel Enhancement Mode Power MOSFET

### Description

The MX6058 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.



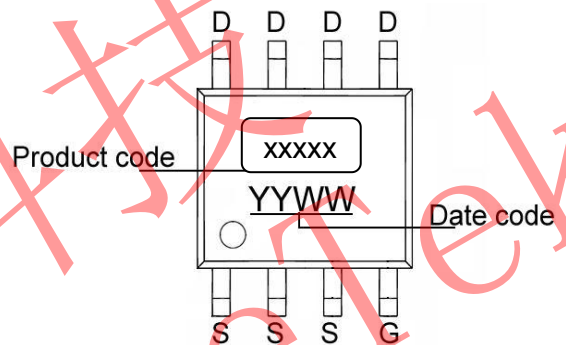
Schematic diagram

### General Features

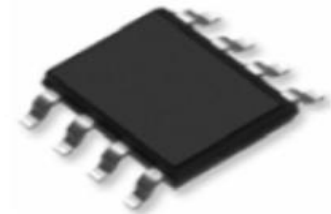
- ◆  $V_{DS} = 60V$ ,  $I_D = 8A$
- ◆  $R_{DS(ON)}(Typ.) = 13m\Omega @ V_{GS} = 10V$
- ◆ High density cell design for ultra low Rds on
- ◆ Fully characterized Avalanche voltage and current

### Application

Power switching application  
Hard Switched and High Frequency Circuits  
Uninterruptible Power Supply



Marking and pin assignment



SOP-8 top view

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	8	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	5.5	A
Pulsed Drain Current	$I_{DM}$	32	A
Maximum Power Dissipation	$P_D$	2.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$



**Electrical Characteristics** (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.4	1.9	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =8A	-	13	16	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =7A	-	80	-	S
<b>Dynamic Characteristics</b> (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, F=1.0MHz	-	2460	-	PF
Output Capacitance	C <sub>oss</sub>		-	163	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	126	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =20V, R <sub>L</sub> =6.7Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	7.4	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	5.1	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	28.2	-	nS
Turn-Off Fall Time	t <sub>f</sub>	V <sub>DS</sub> =20V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	5.5	-	nS
Total Gate Charge	Q <sub>g</sub>		-	50	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	6	-	nC
Gate-Drain Charge	Q <sub>gd</sub>	-	15	-	nC	
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>	-	-	-	50	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =20A	-	28	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs <sup>(Note3)</sup>	-	40	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	50	°C/W
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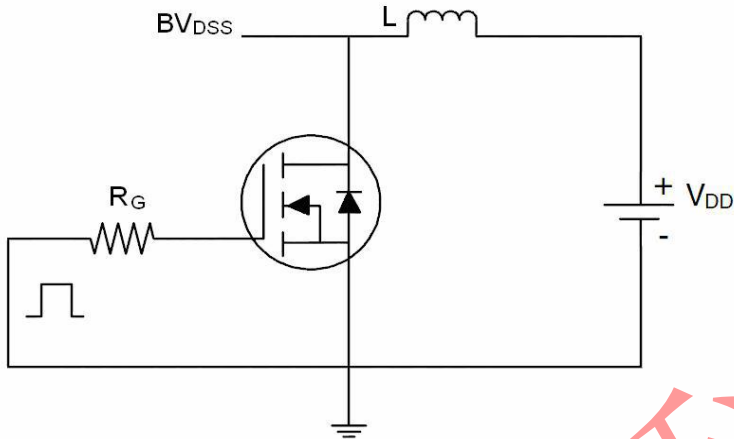
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

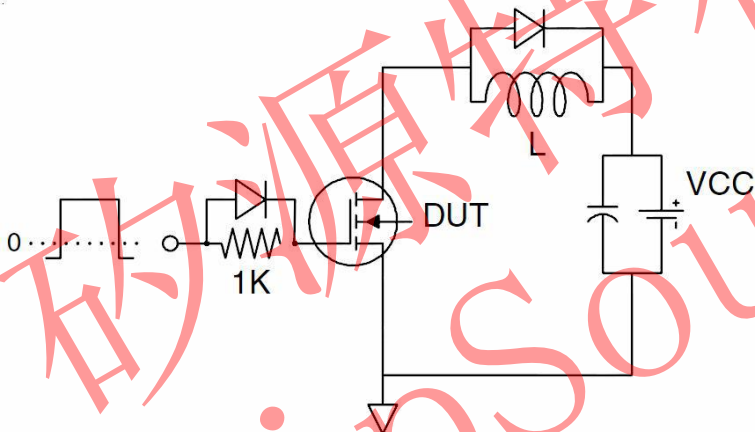


## Test Circuit

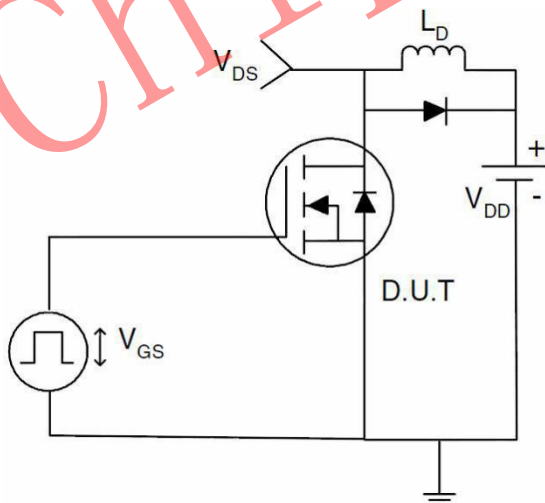
### 1) EAS Test Circuits



### 2) Gate Charge Test Circuit:



### 3) Switch Time Test Circuit:





Typical Electrical and Thermal Characteristics (Curves)

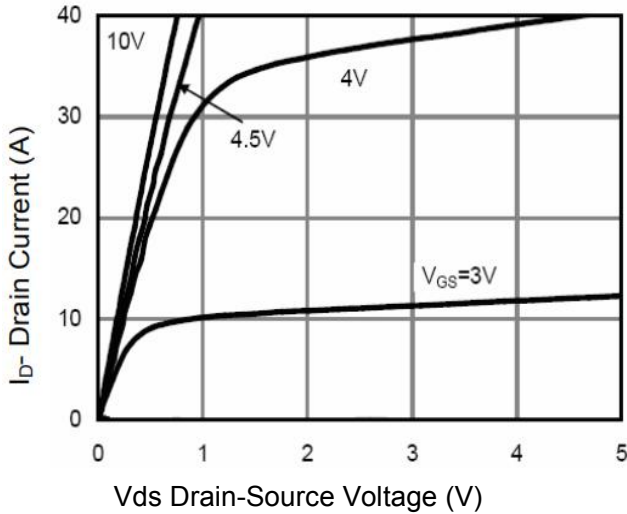


Figure 1 Output Characteristics

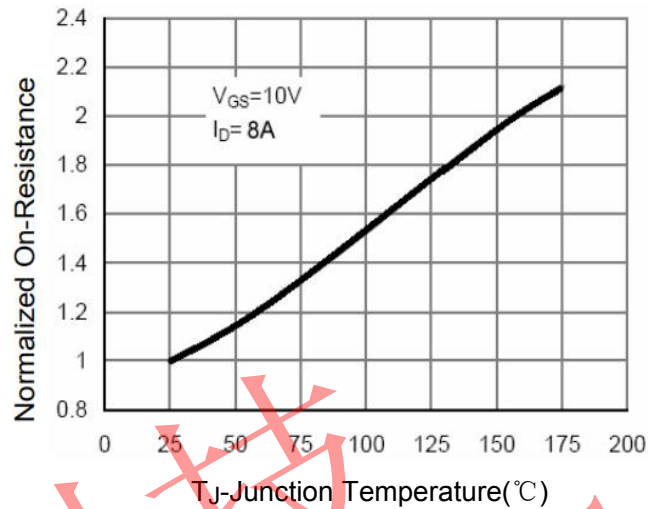


Figure 4 Rdson-Junction Temperature

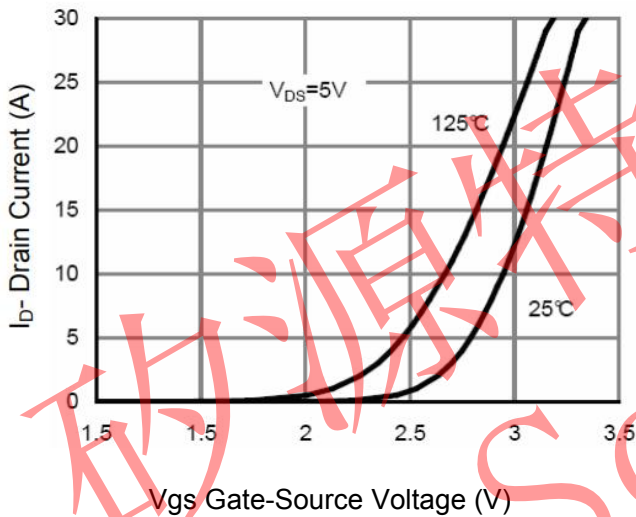


Figure 2 Transfer Characteristics

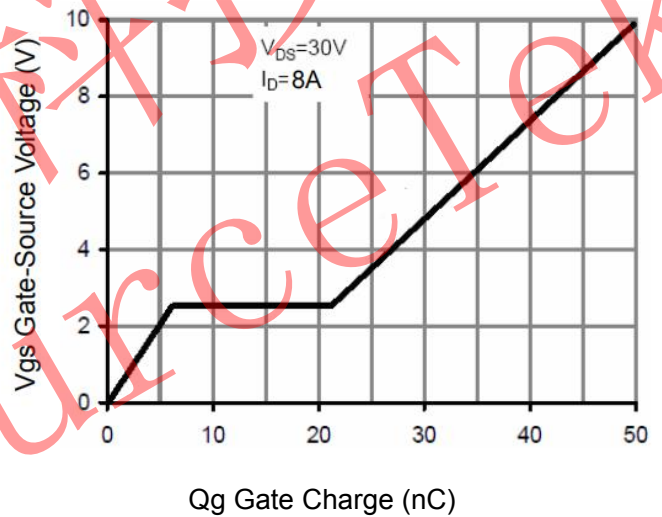
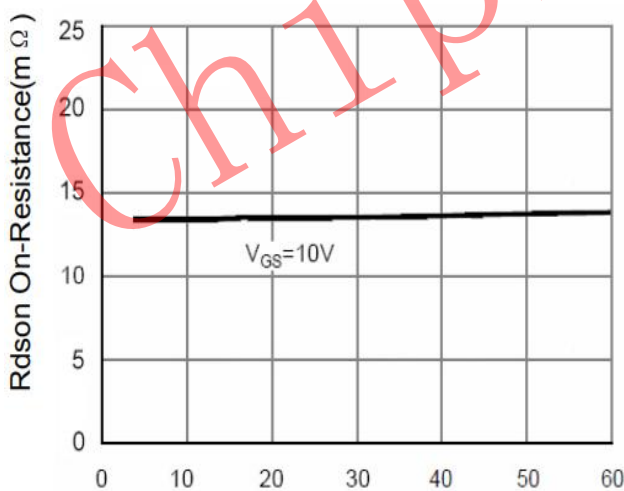
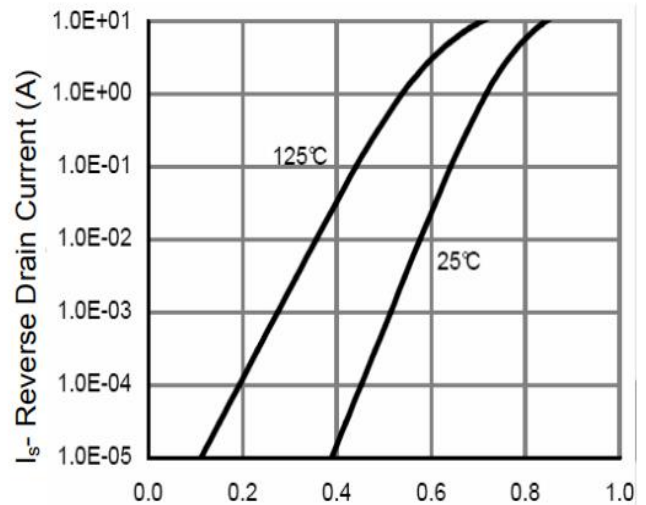


Figure 5 Gate Charge



$I_D$ - Drain Current(A)  
Figure 3 Rdson- Drain Current



$V_{SD}$  Source-Drain Voltage (v)  
Figure 6 Source- Drain Diode Forward

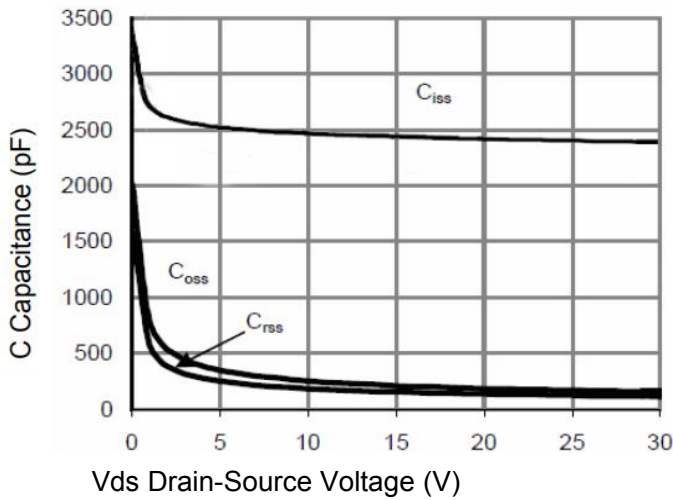


Figure 7 Capacitance vs Vds

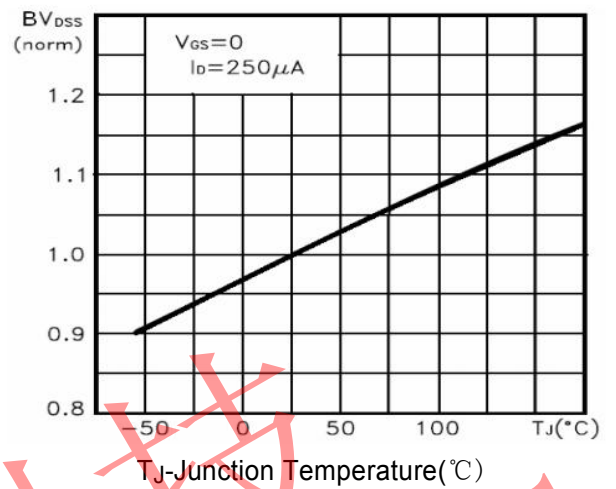


Figure 9 BVdss vs Junction Temperature

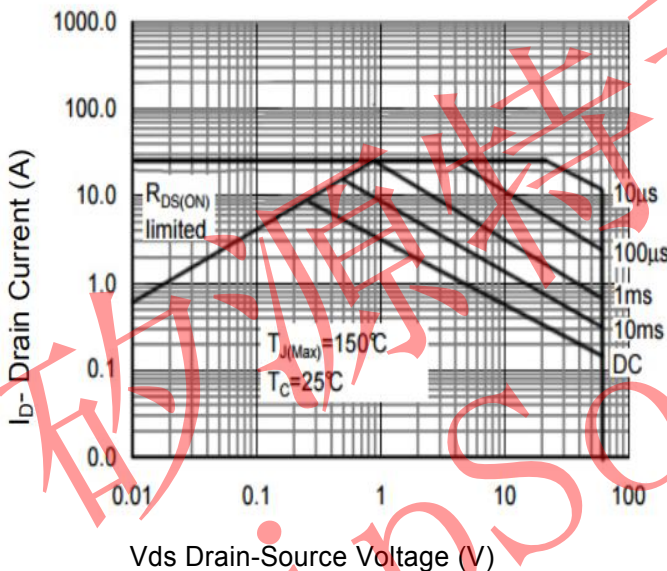


Figure 8 Safe Operation Area

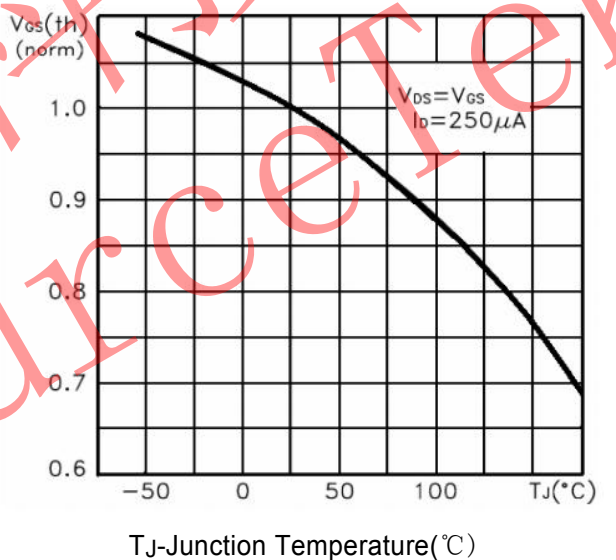


Figure 10 Vgs(th) vs Junction Temperature

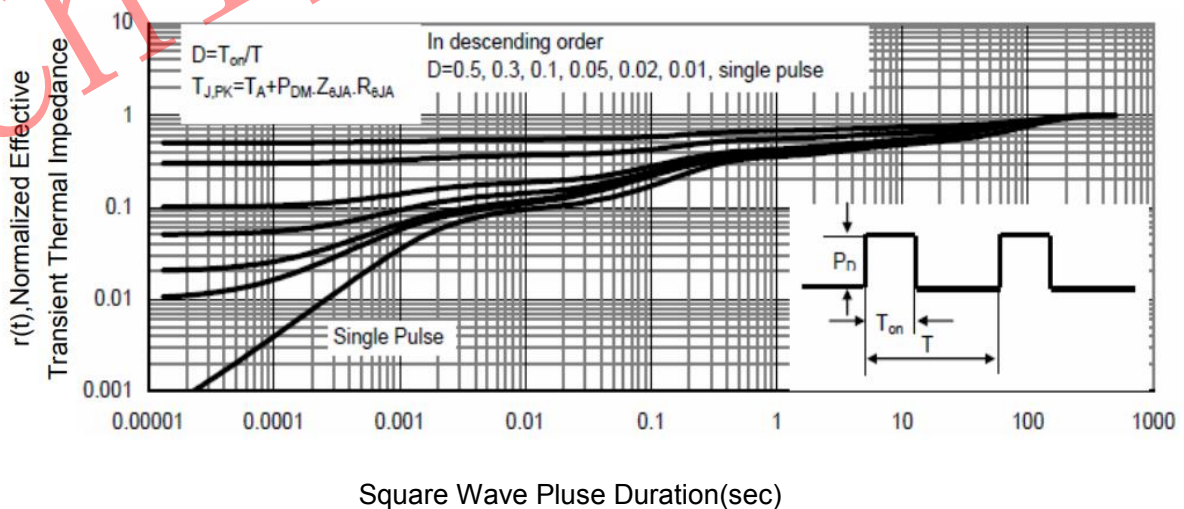
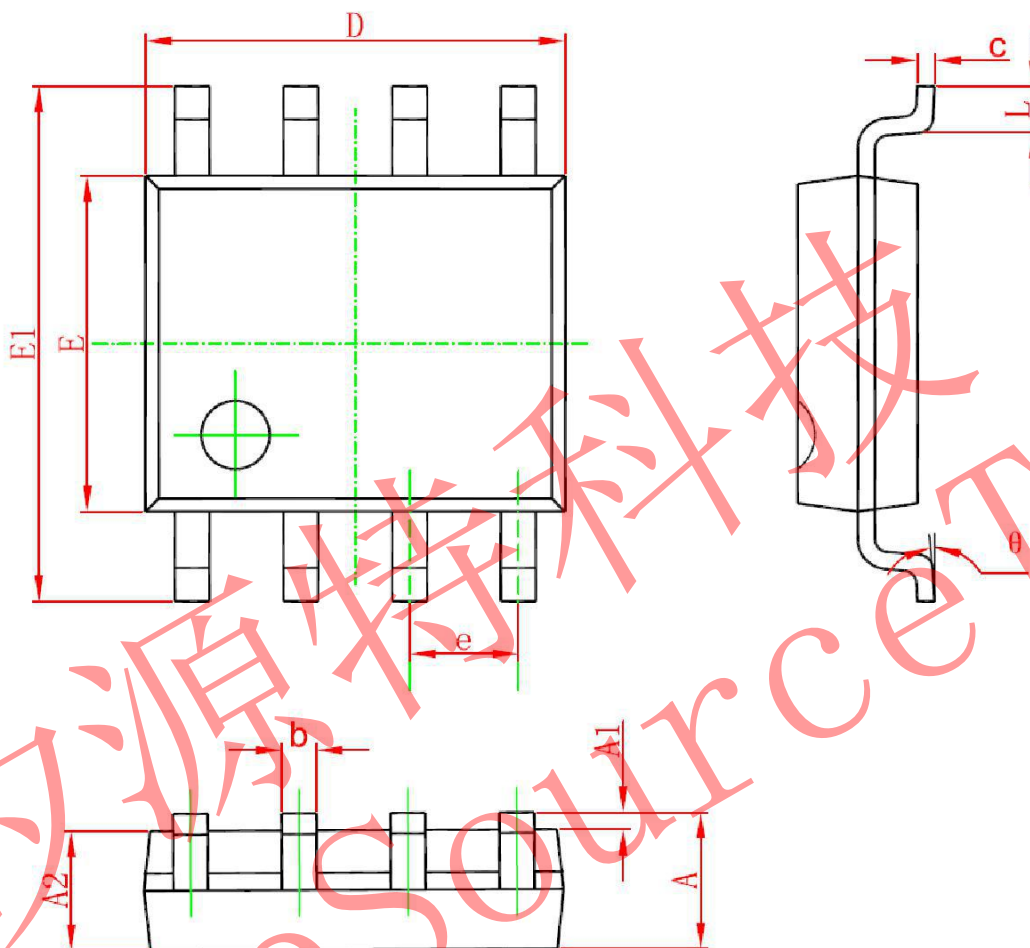


Figure 11 Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°