FM8648M

0.4 to 6.0GHz SP4T Switch with MIPI

Features

- Broadband frequency range: 0.4 to 6.0GHz
- Only one supply voltage needed
- MIPI RFFE V2.1 compatible Interface
- Compact 1.1mm x 1.1mm x 0.5mm LGA-9 package, MSL3

Applications

- 2G/3G/4G/5G antenna TRX switch

Description

The FM8648M is a CMOS silicon-on-insulator (SOI), SP4T transmitting and receiving switch. The high linearity performance and low insertion loss makes the device an ideal choice for GSM/WCDMA/LTE handset and data card applications.

The FM8648M is compatible with MIPI RFFE V2.1 control, which is a key requirement for many cellular transceivers. This part is packaged in a compact 1.1mm x 1.1mm x 0.5mm LGA package, which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

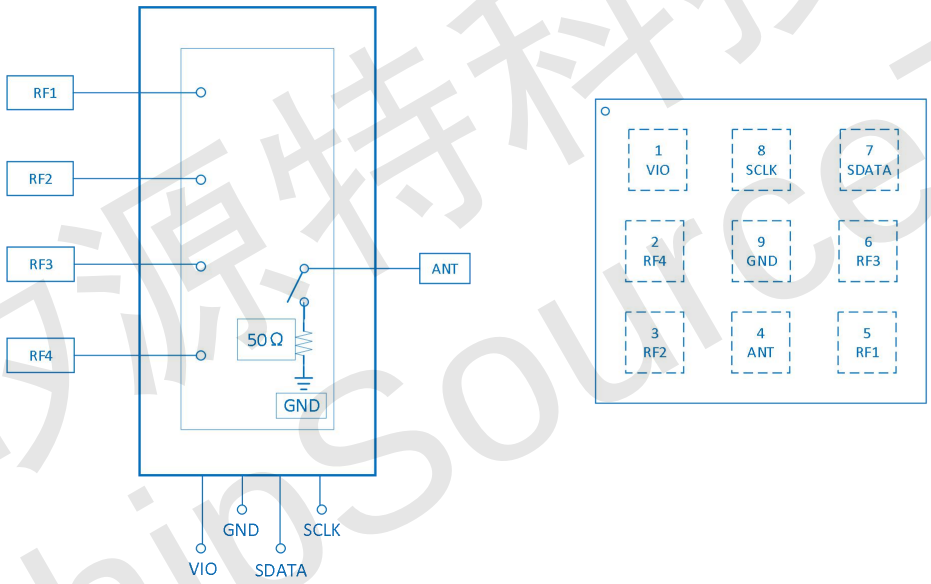


Figure 1. Functional Block Diagram and Pin Configuration Top View

Function Characteristics

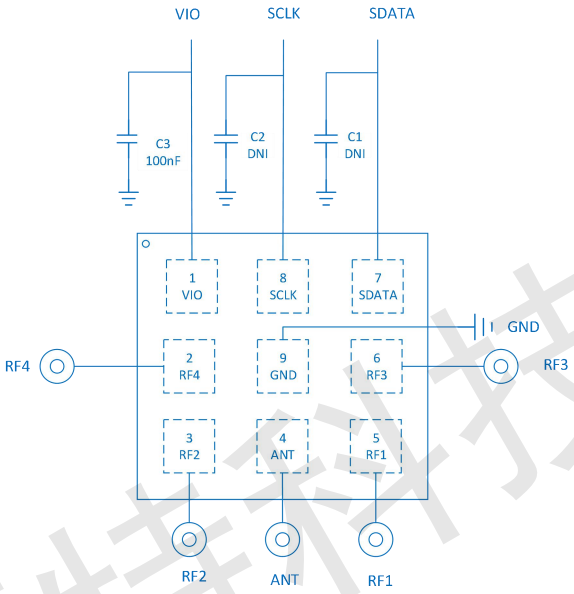


Figure 2. FM8648M Application Circuit

Table 1. Pin Descriptions

NO.	Name	Description	NO.	Name	Description
1	VIO	Supply Voltage	6	RF3	RF Port3
2	RF4	RF Port4	7	SDATA	RFFE Data Bus
3	RF2	RF Port2	8	SCLK	RFFE Clock Bus
4	ANT	Antenna Port	9	GND	Ground
5	RF1	RF Port1			

Table 2. Register_0 Truth Table for RF Operating Modes

Mode				Register_0				
	D7	D6	D5	D4	D3	D2	D1	D0
All RF Paths Isolated	0	0	0	0	0	0	0	0
RF1 ON	0	0	0	0	0	0	0	1
RF2 ON	0	0	0	0	0	0	1	0
RF3 ON	0	0	0	0	0	1	0	0
RF4 ON	0	0	0	0	1	0	0	0

Electrical Characteristics

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{IO}	-0.3	2.5	V	TA=25℃
RFFE Bus Voltage (SDATA, SCLK)	V_I	-0.3	2.5		TA=25℃
Max RF Input Power (ANT to RF1/2/3/4)	P_{IN}		38	dBm	F0=950MHz, 20% DC, VIO=1.8V, ZO=50Ω, TA=25℃
Device Operating Temperature	T_{OP}	-40	90	℃	
Device Storage Temperature	T_{STG}	-55	150		
Electrostatic Discharge(All Pins)	$V_{ESD(HBM)}$	1		kV	Human Body Model
	$V_{ESD(CDM)}$	1			Charged Device Model

Note:

Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Table 4. Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Frequency	F_0	0.4		6.0	GHz
Supply Voltage	V_{IO}	1.65	1.80	1.95	V
RFFE Bus Voltage(SDATA, SCLK) High	V_{IH}	0.8*VIO	VIO	VIO	
RFFE Bus Voltage(SDATA, SCLK) Low	V_{IL}	0	0	0.2*VIO	

Table 5. Nominal Operating Parameters

Parameter	Symbol	Specification			Unit	Condition
		MIN	TYP	MAX		
Normal Condition	V_{IO}=1.8V, V_{IH}=1.8V, V_{IL}=0V, P_{IN}=0dBm, VSWR=1:1, T_A=25℃, Unless Otherwise Stated					
DC Performances						
Supply Current	I_{IO}		80	100	μA	Active State
			6	10		Low Power State
Timing Performances						
Switching Time (One On Path to Another)	T_{SW}		2	3	μs	Switching CMD 50% SCLK to 90%/10% RF
Wakeup Time	T_{WK}		5	10		End of Low Power State 50% SCLK to 90% RF
Turn On Time	T_{ON}			20		Cold Start, 50% VIO to 90% RF
VIO Reset Time	T_{VIO_RST}	10				VIO Off to it starts to re-power up
RF Performances						
Insertion Loss (ANT to RF1/2/3/4)	IL		0.40 0.45 0.50 0.55 0.65	0.45 0.50 0.55 0.65 0.90	dB	F_0=0.4 to 1.0GHz F_0=1.0 to 2.0GHz F_0=2.0 to 3.0GHz F_0=3.0 to 3.8GHz F_0=4.8 to 6.0GHz
Isolation (ANT to RF1/2/3/4)	ISO	40 38 33 28 21	42 40 35 30 24			F_0=0.4 to 1.0GHz F_0=1.0 to 2.0GHz F_0=2.0 to 3.0GHz F_0=3.0 to 3.8GHz F_0=4.8 to 6.0GHz
Input Return Loss (ANT to RF1/2/3/4)	RL	12 10	15 13			F_0=0.4 to 2.7GHz F_0=2.7 to 6.0GHz
Input 0.1dB Compression Point (ANT to RF1/2/3/4)	$P_{0.1dB}$		38		dBm	F_0=950MHz, 20% DC
2nd Order Harmonic (ANT to RF1/2/3/4)	$2F_0$		-90 -85 -85	-85 -80 -80	dBc	F_0=950MHz @26dBm F_0=950MHz @35dBm F_0=1800MHz @32dBm
3rd Order Harmonic (ANT to RF1/2/3/4)	$3F_0$		-92 -85 -85	-88 -80 -80		F_0=950MHz @26dBm F_0=950MHz @35dBm F_0=1800MHz @32dBm

MIPI RFFE Read and Write Timing

MIPI RFFE supports the following Command Sequences:

- Register Write
- Register Read
- Register_0 Write

Figure 3 and Figure 4 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 5 describes the Register_0 write command sequence. In the below timing figures, SA[3:0] is the slave address. A[4:0] is the register address. D[7:0] is the data. “P” is a parity bit.

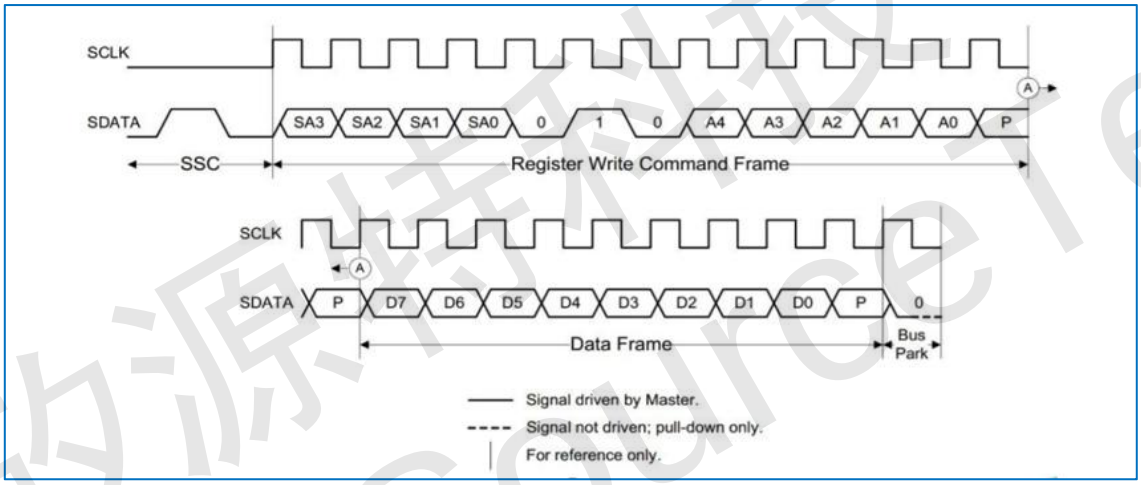


Figure 3 Register Write Command Sequence

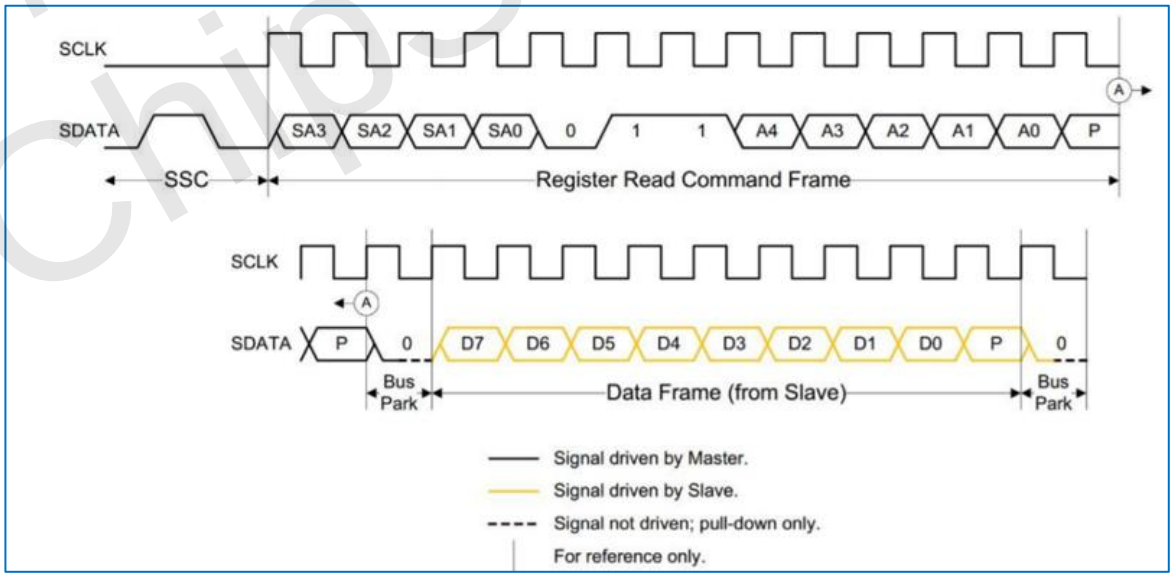


Figure 4 Register Read Command Sequence

Figure 5 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and a only seven- bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle.

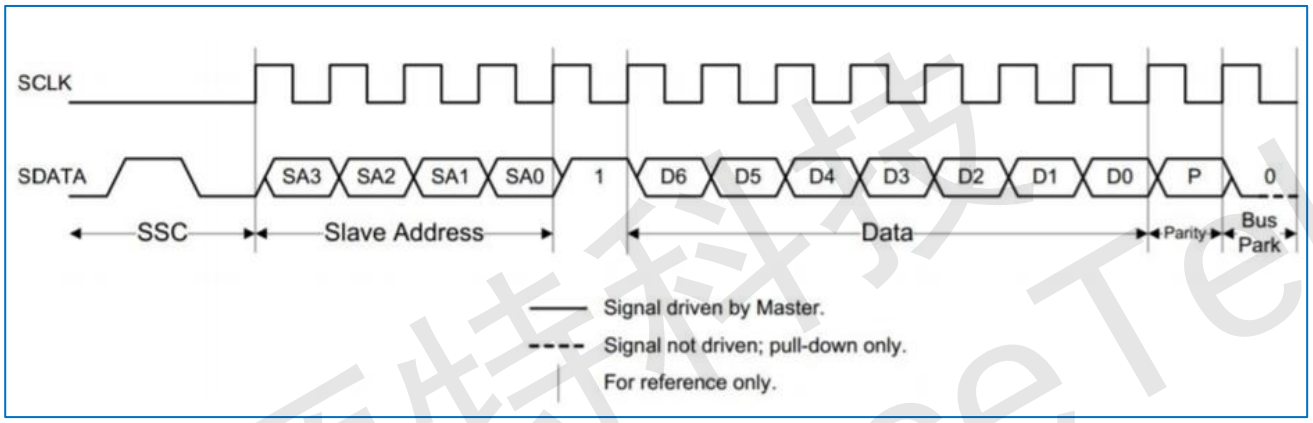


Figure 5 Register_0 Write Command Sequence

Other information such as MIPI RFFE USID programming sequence, MIPI RFFE bus specifications, etc. can be referred to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V2.1.

Register Definition

Table 6. Register Definition Table

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x00	REGISTER_0	7:0	R/W	RF Control	Register_0 truth Table: Table 2	0x00	No	Yes
0x1C	PM_TRIG	7	R/W	PWR_MODE_1	0b0: Normal Operation Mode Write Value:0b0, Read Value:0b0 0b1: Low Power Mode Write Value:0b1, Read Value:0b1	0b0	Yes	No
		6	R/W	PWR_MODE_0	0b0: Normal Operation (ACTIVE) 0b1: Reset all registers to default settings (STARTUP) Write value: 0b1, Read Value: 0b0	0b0		
		5	R/W	Trigger_Mask_2	0b0: Trigger_2 enabled 0b1: Trigger_2 disabled	0b0	No	No
		4	R/W	Trigger_Mask_1	0b0: Trigger_1 enabled 0b1: Trigger_1 disabled	0b0	No	No
		3	R/W	Trigger_Mask_0	0b0: Trigger_0 enabled 0b1: Trigger_0 disabled	0b0	No	No
		Note: If any one of the three Trigger Masks is set to a logic '1' the corresponding Trigger is disabled, in that case data written to a register associated with the Trigger goes directly to the destination register. Otherwise, if the Trigger Mask is enabled (via a logic '0'), incoming data is written to the shadow register, and the destination register is unchanged until its corresponding Trigger is asserted.						
		2	W	Trigger_2	0b0: Keep its associated destination registers unchanged 0b1: Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_2 is	0b0	Yes	No

					disabled(Logic '0')			
		1	W	Trigger_1	0b0: Keep its associated destination registers unchanged 0b1: Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_1 is disabled(Logic '0')	0b0	Yes	No
		0	W	Trigger_0	0b0: Keep its associated destination registers unchanged 0b1: Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_0 is disabled(Logic '0')	0b0	Yes	No
0x1D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x72	No	No
0x1E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x78	No	No
0x1F	MAN_USID	7:6	R	RESERVED		0b00	No	No
		5:4	R	MANUFACTURER_ID[9:8]	Upper two bits of MIPI registered Manufacturer ID	0x2	No	No
		3:0	R/W	USID	Unique Slave Address	0x8	No	No

MIPI RFFE Operating Sequences

Here are some recommendations for MIPI RFFE operating sequences to prevent the device from damage.

1) Basic Operational Sequences

- Power On -- Apply Supply (VIO)-> Apply MIPI RFFE Bus (SCLK & SDATA) -> Apply RF Signal
- Power Off -- Remove RF Signal-> Remove MIPI RFFE Bus (SCLK & SDATA)->Remove Supply (VIO)

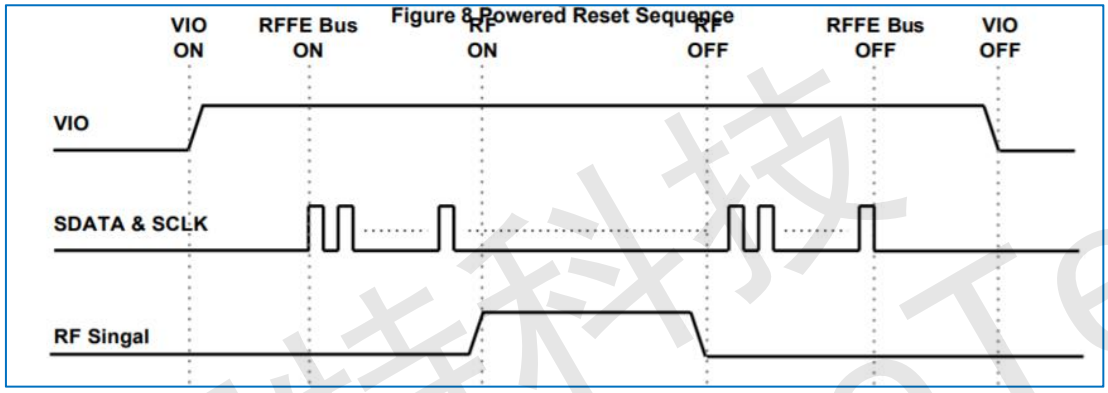


Figure 6 Basic Power On and Power Off Sequence

2) There shall be at least TON before RF power can be applied to any RF Path

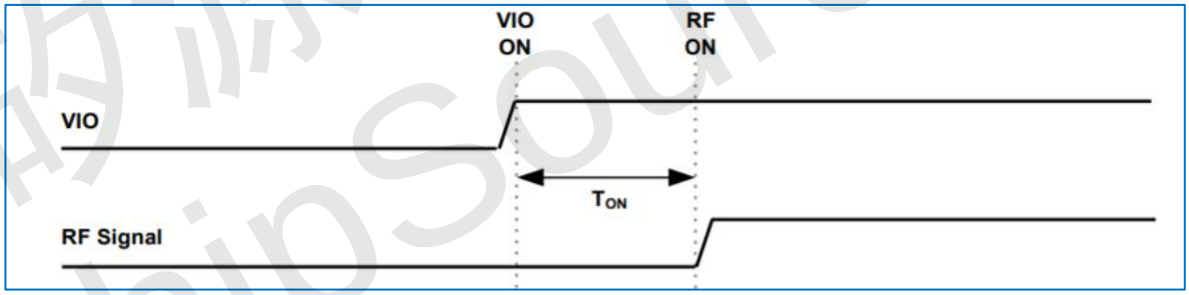


Figure 7 Supply and RF Signal On Sequence

3) Once VIO is off, there shall be at least TRST before VIO is allowed to repower on again.

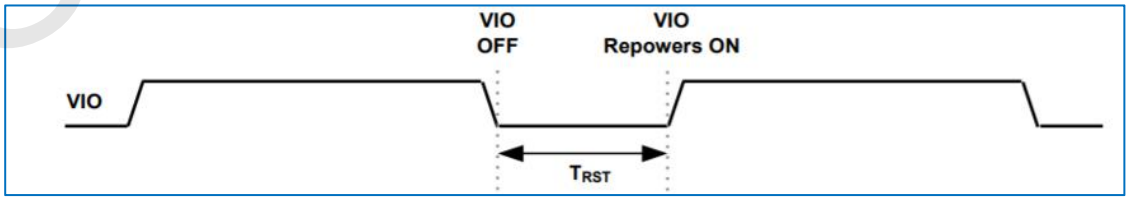


Figure 8 Supply and RF Signal On Sequence

4) If RF signal is to be switched from one RF path to another or some paths to others, RF signal shall not be applied during such switching events to protect the devices. Hence, RF signal shall be removed before the switching command is implemented. RF signal shall not be applied before waiting at least TSW.

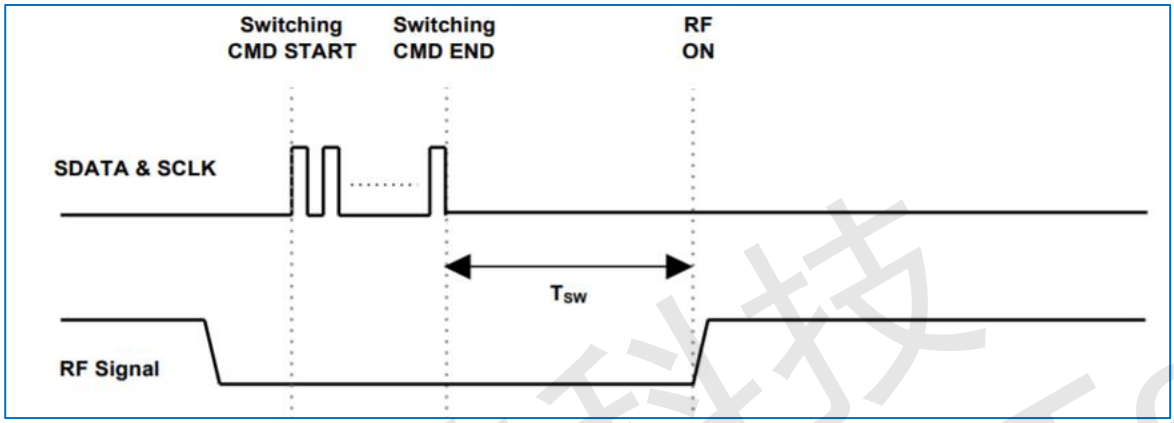


Figure 9 RF Path Switching Sequence

5) RF Signal shall not be applied during low power state. Hence, RF signal shall be removed before device enters low power state. After the state is switched from low power to active, there shall be at least TWK before the RF signal can be applied

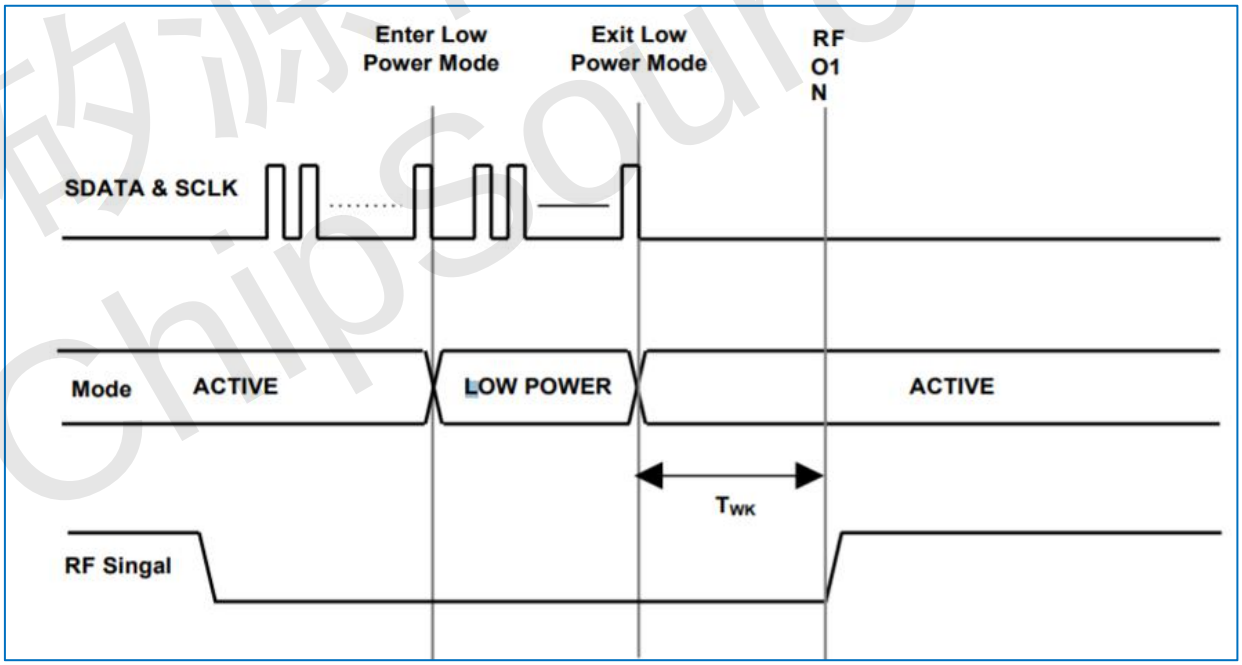
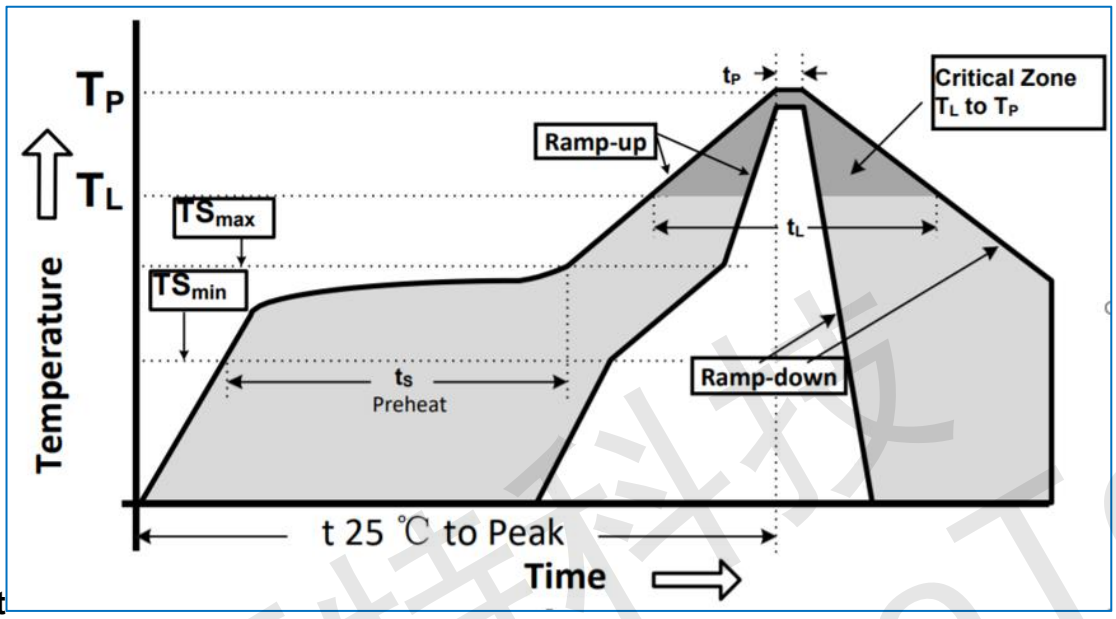


Figure 10 Enter and Exit Low Power State Sequence

Reflow



Chart

Figure 11 Recommended Lead-Free Reflow Profile

Table 7. Reflow Chart Parameters

Reflow Profile	Parameter
Preheat Temperature(TSMIN to TSMAX)	150℃ to 200℃
Preheat Time(ts)	60 to 180 Seconds
Ramp-Up Rate(TSMAX to TP)	3℃/s MAX
Time Above TL 217℃(tL)	60 to 150 Seconds
Peak Temperature (TP)	260℃
Time within 5℃ of Peak Temperature(tP)	20 to 40 Seconds
Ramp-Down Rate(TSMAX to TP)	6℃/s MAX
Time for 25℃ to Peak Temperature(t25-TP)	8 Minutes MAX

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.