DRV883x 低压 H 桥驱动器

1 特性

- H 桥电机驱动器
  - 驱动一个直流电机或其他负载
  - 低金属氧化物半导体场效应晶体管 (MOSFET) 导通电阻：高侧 + 低侧 (HS + LS) 280mΩ
- 1.8A 最大驱动电流
- 独立的电机和逻辑电源引脚：
  - 电机 VM：0 至 11V
  - 逻辑 VCC：1.8 至 7V
- 脉宽调制 (PWM) 或 PH/EN 接口
  - DRV8837：脉宽调制 (PWM)，IN1/IN2
  - DRV8838：PH/EN
- 具有 120nA 最大睡眠电流的低功耗睡眠模式
  - nSLEEP 引脚
- 小型封装尺寸
  - 8 超薄小外形尺寸封装 (WSON) (PowerPAD™)
  - 2.0mm × 2.0mm
- 保护特性
  - VCC 欠压闭锁 (UVLO)
  - 过流保护 (OCP)
  - 热关断 (TSD)

2 应用范围

- 摄像机
- 数字单镜头反光 (DSLR) 镜头
- 消费类产品
- 玩具
- 机器人技术
- 医疗设备

3 说明

DRV883x 为摄像机、消费类产品、玩具和其它低电压或者电池供电的运动控制类应用提供了一个集成的电机驱动器解决方案。 此器件能够驱动一个直流电机或其他诸如螺线管的器件。 输出驱动器块由一个配置为 H 桥的 N 通道功率 MOSFET 组成，以驱动电机绕组。一个内部电荷泵生成所需的栅极驱动电压。

DRV883x 能够提供高达 1.8A 的输出电流。 它运行在 0 至 11V 之间的电机电源电压，以及 1.8V 至 7.0V 范围内的器件电源电压上。

DRV8837 具有一个 PWM (IN/IN) 输入接口；DRV8837 具有一个 PH/EN 输入接口（此处应为 DRV8838 具有一个 PH/EN 输入接口）。 这两个接口都与行业标准器件兼容。

还提供用于过流保护、短路保护、欠压闭锁和过热保护的内部关断功能。

器件信息

订货编号	封装	封装尺寸
DRV8837DSGR	WSON (8)	2.0mm x 2.0mm
DRV8838DSGR	WSON (8)	2.0mm x 2.0mm

DRV883x

1.8 to 7 V   0 to 11 V
VCC ↓   ↓ VM

Controller — PWM or PH and EN →
Controller — nSLEEP →

DRV8837 and DRV8838
Brushed DC Motor Driver

1.8 A   M

目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (December 2013) to Revision C	Page
• 已添加 DRV8838 器件信息、技术规格和时序图..	1
• 已添加器件信息表	1
• 已添加一个 PWM 接口图	1
• Added more information to the Detailed Description and moved information from the Functional Description	9
• Added functional block diagram for DRV8838	10
• Added the Applications and Implementation section	13
• Added Power Supply Recommendations, Layout, Device and Documentation Support, and Packaging sections.............	15

Changes from Revision A (August 2012) to Revision B	Page
• 已更改 特性部分..	1
• Changed Recommended Operating Conditions...	4
• Changed Electrical Characteristics section	5
• Changed Timing Requirements section	6
• Changed Power Supplies and Input Pins section	11

5 Terminal Configuration and Functions

DRV8837 DSG – WSON
(Top View)

```
        ┌─────────┐
VM    1 │         │ 8   VCC
OUT1  2 │  GND    │ 7   nSLEEP
OUT2  3 │ (PPAD)  │ 6   IN1
GND   4 │         │ 5   IN2
        └─────────┘
```
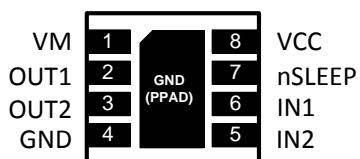
DRV8838 DSG – WSON
(Top View)

```
        ┌─────────┐
VM    1 │         │ 8   VCC
OUT1  2 │  GND    │ 7   nSLEEP
OUT2  3 │ (PPAD)  │ 6   PH
GND   4 │         │ 5   EN
        └─────────┘
```
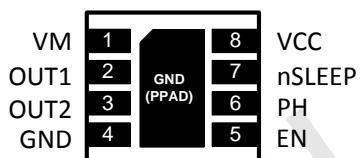
Terminal Descriptions

TERMINAL		TYPE	DESCRIPTION
NAME	**NUMBER**		
POWER AND GROUND			
GND	4	PWR	Device ground Must be connected to ground
VCC	8	PWR	Logic Power supply Bypass to GND with a 0.1-μF ceramic capacitor rated for VCC
VM	1	PWR	Motor power supply Bypass to GND with a 0.1-μF ceramic capacitor rated for VM
CONTROL			
IN1/PH	6	I	IN1 or PHASE input See Detailed Description for more information
IN2/EN	5	I	IN2 or ENABLE input
nSLEEP	7	I	Sleep mode input Logic low puts the device in low-power sleep mode; logic high for normal operation; internal pulldown resistor
OUTPUT			
OUT1	2	O	Motor output
OUT2	3	O	Connect to motor winding

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)](2)

	MIN	MAX	UNIT
Motor power supply voltage range (VM)	−0.3	12	V
Logic power supply voltage range (VCC)	−0.3	7	V
Control pin voltage range (IN1, IN2, PH, EN, nSLEEP)	−0.5	7	V
Peak drive current (OUT1, OUT2)	Internally limited		A
T_J, operating virtual junction temperature range	−40	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 Handling Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	−60	150	ºC

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
VM	Motor power supply voltage range	0	11	V
VCC	Logic power supply voltage range	1.8	7	V
I_{OUT}	Motor peak current	0	1.8	A
f_{PWM}	Externally applied PWM frequency	0	250	kHz
V_{LOGIC}	Logic level input voltage	0	5.5	V
T_A	Operating ambient temperature	−40	85	°C

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

	THERMAL METRIC[(1)]	DRV8837, DRV8838 WSON (8 TERMINALS)	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance[(2)]	60.9	°C/W
$\Theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance[(3)]	71.4	
Θ_{JB}	Junction-to-board thermal resistance[(4)]	32.2	
Ψ_{JT}	Junction-to-top characterization parameter[(5)]	1.6	
Ψ_{JB}	Junction-to-board characterization parameter[(6)]	32.8	
$\Theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance[(7)]	9.8	

(1) For more information about traditional and new thermal limits, see the IC Package Thermal Metrics Report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VCC)						
VM	VM operating voltage		0		11	V
I_{VM}	VM operating supply current	VM = 5 V; VCC = 3 V; No PWM		40	100	µA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		30	95	nA
VCC	VCC operating voltage		1.8		7	V
I_{VCC}	VCC operating supply current	VM = 5 V; VCC = 3 V; No PWM		300	500	µA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.7	1.5	mA
I_{VCCQ}	VCC sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		5	25	nA
CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP)						
V_{IL}	Input logic low voltage		0.25 × VCC	0.38 × VCC		V
V_{IH}	Input logic high voltage			0.46 × VCC	0.5 × VCC	V
V_{HYS}	Input logic hysteresis			0.08 × VCC		mV
I_{IL}	Input logic low current	V_{IN} = 0 V	−5		5	µA
I_{IH}	Input logic high current	V_{IN} = 3.3 V			50	µA
		V_{IN} = 3.3 V, DRV8838 nSLEEP pin		60		µA
R_{PD}	Pulldown resistance			100		kΩ
		DRV8838 nSLEEP pin		55		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	HS + LS FET on-resistance	VM = 5 V; VCC = 3 V; I_O = 800 mA; T_J = 25°C		280	330	mΩ
I_{OFF}	Off-state leakage current	V_{OUT} = 0 V	−200		200	nA
PROTECTION CIRCUITS						
V_{UVLO}	VCC undervoltage lockout	VCC falling			1.7	V
		VCC rising			1.8	
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{DEG}	Overcurrent deglitch time			1		µs
t_{RETRY}	Overcurrent retry time			1		ms
T_{TSD}	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C

6.6 Timing Requirements

T_A = 25°C, VM = 5 V, VCC = 3 V, RL = 20 Ω

NUMBER	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
1	t_1	Delay time, PHASE high to OUT1 low		160	ns
2	t_2	Delay time, PHASE high to OUT2 high		200	ns
3	t_3	Delay time, PHASE low to OUT1 high		200	ns
4	t_4	Delay time, PHASE low to OUT2 low		160	ns
5	t_5	Delay time, ENBL high to OUTx high		200	ns
6	t_6	Delay time, ENBL low to OUTx low		160	ns
7	t_7	Output enable time		300	ns
8	t_8	Output disable time		300	ns
9	t_9	Delay time, INx high to OUTx high		160	ns
10	t_{10}	Delay time, INx low to OUTx low		160	ns
11	t_{11}	Output rise time	30	188	ns
12	t_{12}	Output fall time	30	188	ns
	t_{wake}	Wake time, nSLEEP rising edge to part active		30	µs
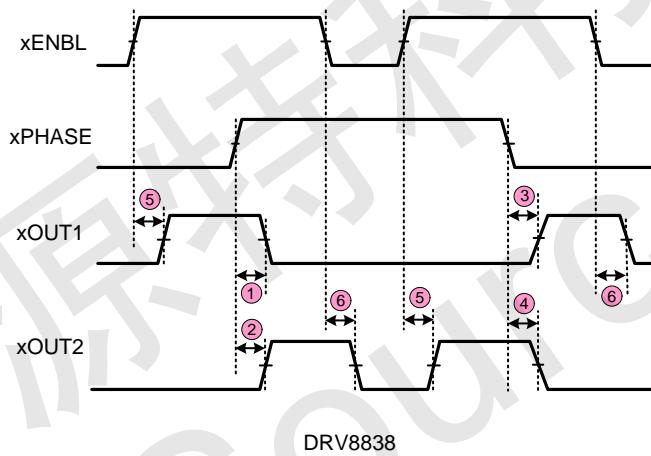
DRV8838

Figure 1. Input and Output Timing for DRV8838
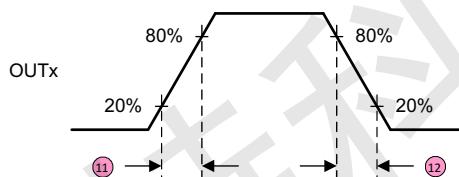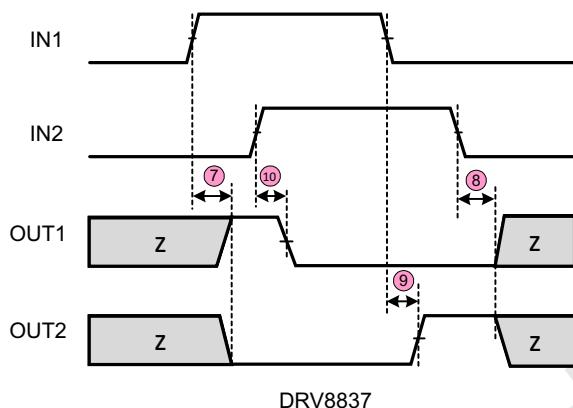
Figure 2. Input and Output Timing for DRV8837

6.7 Typical Characteristics

Plot generated using characterization data

Figure 3. HS + LS R_DS(ON) vs T_A
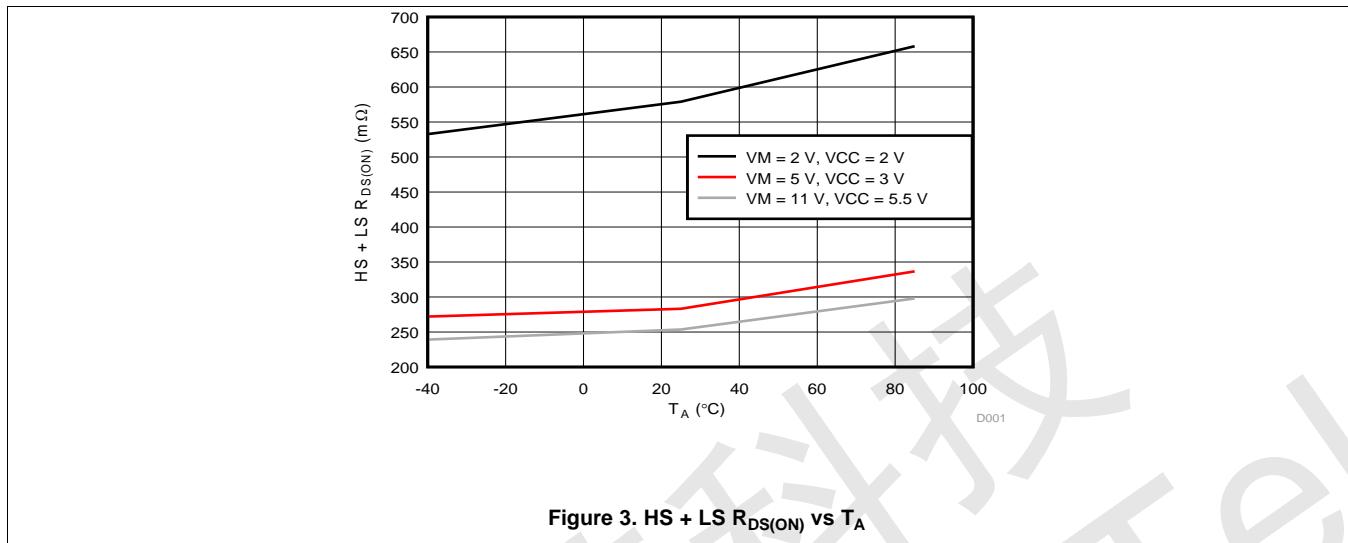
7 Detailed Description

7.1 Overview

The DRV883x is a H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using either a PWM interface (IN1/IN2) on the DRV8837 or a PH/EN interface on the DRV8838.

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

These devices greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV883x adds protection features above traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram
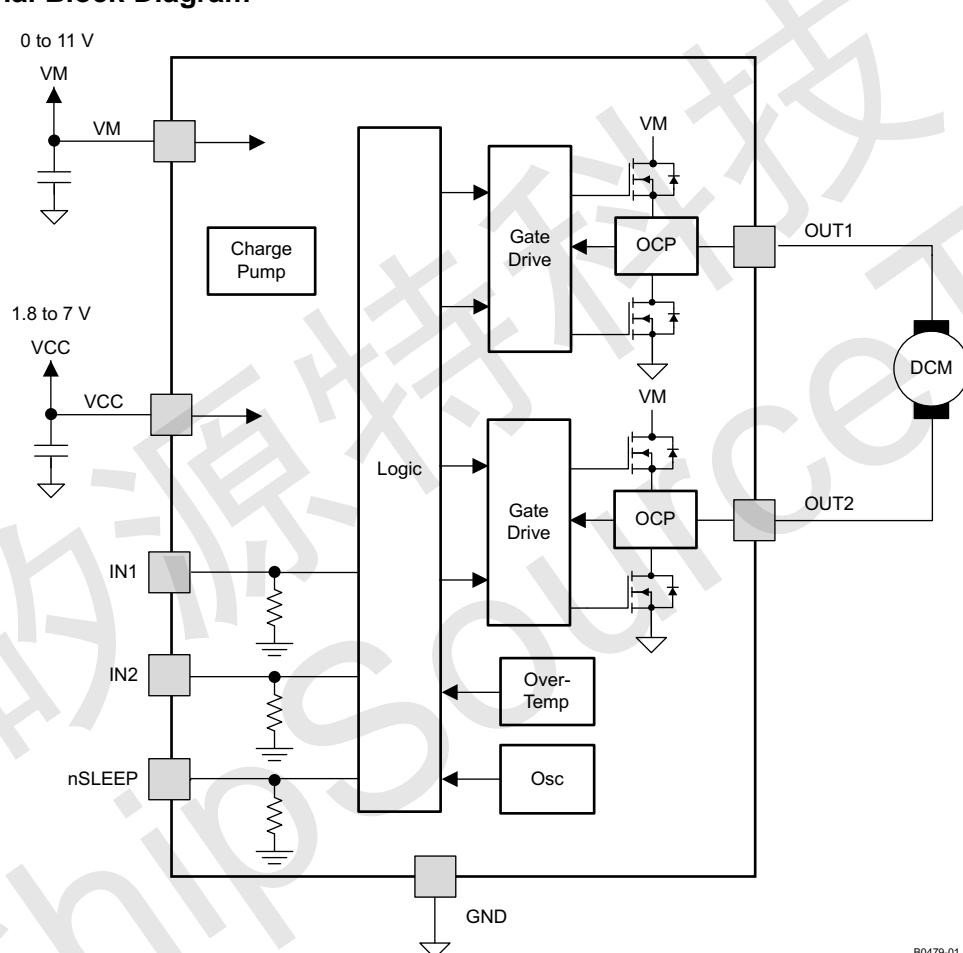
Figure 4. DRV8837 Functional Block Diagram

Functional Block Diagram (continued)
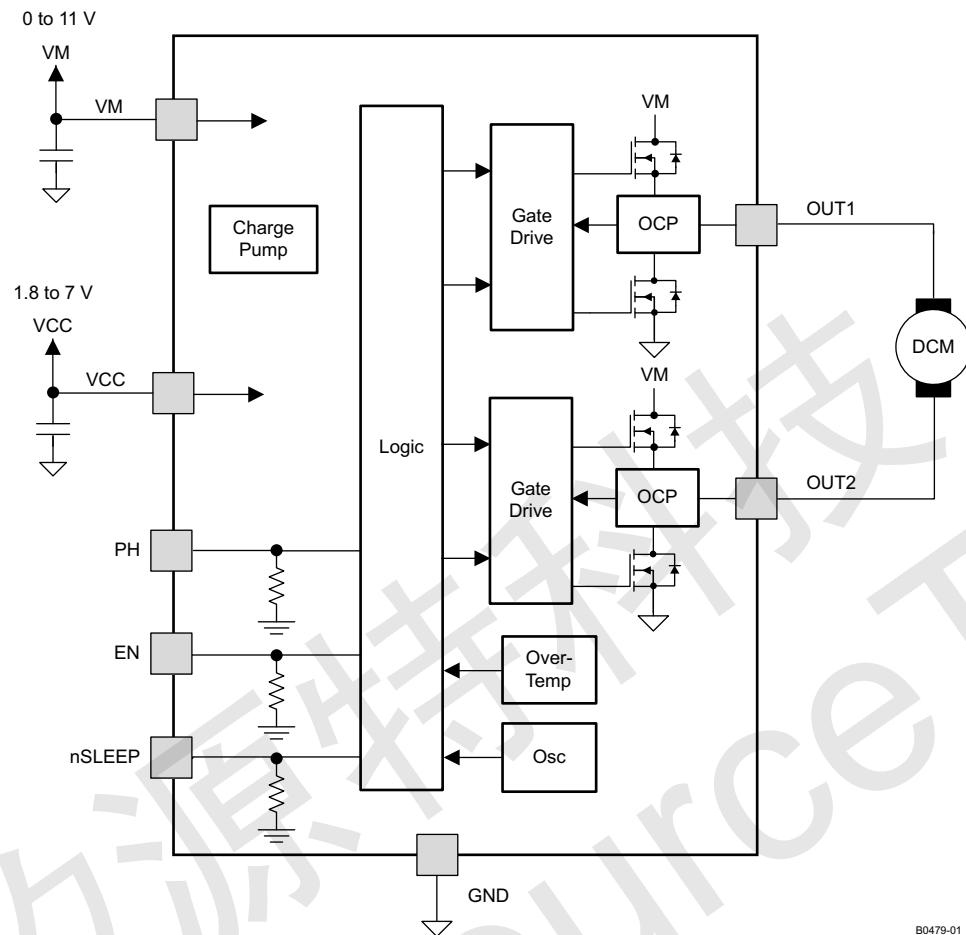
Figure 5. DRV8838 Functional Block Diagram

7.3 Feature Description

7.3.1 Bridge Control

The DRV8837 is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

Table 1 shows the logic for the DRV8837 device:

Table 1. DRV8837 Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	Function (DC Motor)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

The DRV8838 is controlled using a PHASE/ENABLE interface. This interface uses one pin to control the H-bridge current direction, and one pin to enable or disable the H-bridge.

Table 2 shows the logic for the DRV8838:

Table 2. DRV8838 Device Logic

nSLEEP	PH	EN	OUT1	OUT2	Function (DC Motor)
0	X	X	Z	Z	Coast
1	X	0	L	L	Brake
1	1	1	L	H	Reverse
1	0	1	H	L	Forward

7.3.2 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV883x enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.3 Power Supplies and Input Terminals

The input pins may be driven within their recommended operating conditions with or without the VCC and/or VM power supplies present. No leakage current path will exist to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin.

VCC and VM may be applied and removed in any order. When VCC is removed, the device will enter a low power state and draw very little current from VM. VCC and VM may be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage lockout protection (UVLO), so as long as VCC > 1.8 V; the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

7.3.4 Protection Circuits

The DRV883x is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC Undervoltage Lockout: If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VCC rises above the UVLO threshold.

Overcurrent Protection (OCP): An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than tDEG, all FETs in the H-bridge will be disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions will be detected on both the high-side and low-side devices. A short to VM, GND, or from OUT1 to OUT2 results in an overcurrent condition

Thermal Shutdown (TSD): If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 3. Fault Behavior

Fault	Condition	H-bridge	Recovery
VCC undervoltage (UVLO)	VCC < 1.7 V	Disabled	VCC > 1.8 V
Overcurrent (OCP)	I_{OUT} > 1.9 A (MIN)	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	T_J > 150°C (MIN)	Disabled	T_J < 150°C

7.4   Device Functional Modes

The DRV883x is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The DRV883x is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 4. Operation Modes

Mode	Condition	H-bridge
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled

8 Applications and Implementation

8.1 Application Information

The DRV883x is device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the DRV883x.

8.2 Typical Applications
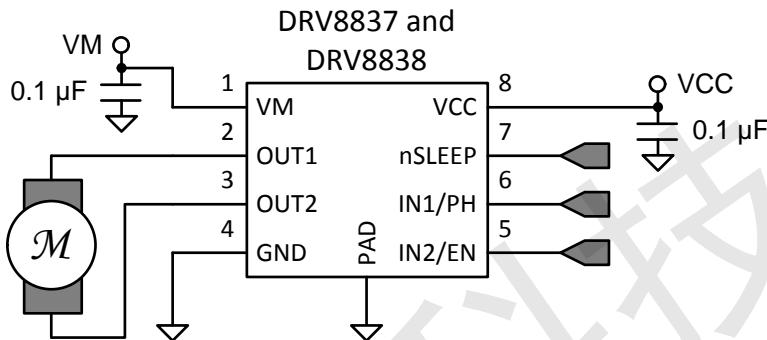
Figure 6. Schematic of DRV883x Application

8.2.1 Design Requirements

Table 5 shows required parameters for a typical usage case.

Table 5. System Design Requirements

Design Parameter	Reference	Example Value
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target RMS current	I_{OUT}	0.8 A

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation

Power dissipation in the DRV883x is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the RMS or DC output current being supplied to the load   (1)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

The DRV883x has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### 8.2.3 Application Performance Plots
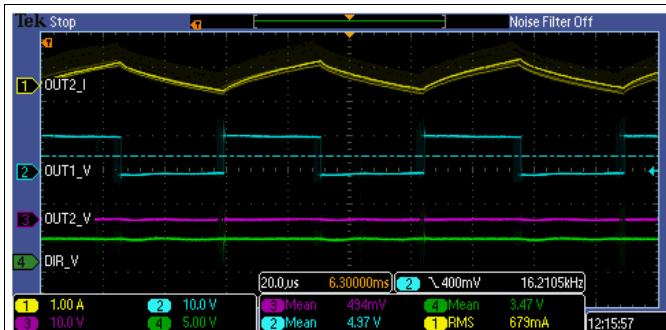

Figure 7. 50% Duty Cycle, Forward Direction

Figure 8. 50% Duty Cycle, Reverse Direction


Figure 9. 20% Duty Cycle, Forward Direction

Figure 10. 20% Duty Cycle, Reverse Direction

9 Power Supply Recommendations

VCC and VM may be applied and removed in any order. When VCC is removed, the device enters a low power state and draws very little current from VM. VCC and VM may be connected together if the supply voltage is between 1.8 and 7 V.

Bypass VM and VCC with 0.1-µF ceramic capacitors rated for VM and VCC. Place these capacitors as close to the device as possible.

The VM voltage supply does not have any undervoltage lockout protection, so as long as VCC > 1.8 V; the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V; however, the load may not be sufficiently driven at low VM voltages.

10 Layout

10.1 Layout Guidelines

The VM and VCC terminals should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for VM and VCC. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

10.2 Layout Example
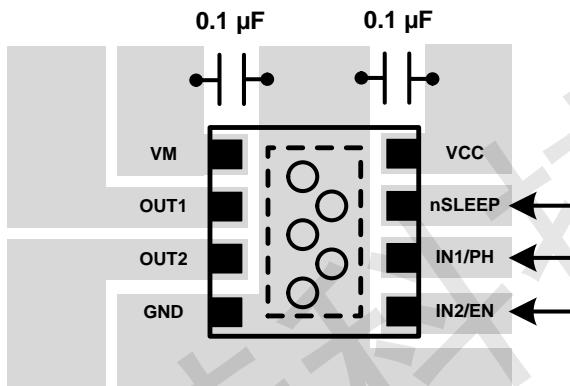
Figure 11. Simplified Layout Example

11 Device and Documentation Support

11.1 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8837	Click here	Click here	Click here	Click here	Click here
DRV8838	Click here	Click here	Click here	Click here	Click here

11.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. ChipSourceTek recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.3 Glossary

SLYZ022 — *TI Glossary*.

   This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧导航栏。

重要声明

深圳市矽源特科技有限公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的ChipSourceTek销售条款与条件。

ChipSourceTek保证其所销售的组件的性能符合产品销售时 ChipSourceTek半导体产品销售条件与条款的适用规范。仅在ChipSourceTek 保证的范围内, 且 ChipSourceTek认为 有必要时才会使 用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

ChipSourceTek对应用帮助或客户产品设计不承担任何义务。客户应对其使用ChipSourceTek组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险, 客户应提供充分的设计与操作安全措施。

ChipSourceTek不对任何ChipSourceTek专利权、版权、屏蔽作品权或其它与使用了ChipSourceTek组件或服务的组合设备、机器或流程相关的 ChipSourceTek知识产权中授予 的直接或隐含权 限作出任何保证或解释。ChipSourceTek所发布的与第三方产品或服务有关的信息, 不能构成从ChipSourceTek获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是ChipSourceTek的专利权或其它 知识产权方面的许可。

对于ChipSourceTek的产品手册或数据表中ChipSourceTek信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行 复制。ChipSourceTek对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售ChipSourceTek组件或服务时, 如果对该组件或服务参数的陈述与ChipSourceTek标明的参数相比存在差异或虚假成分, 则会失去相关ChipSourceTek 组件 或服务的所有明 示或暗示授权, 且这是不正当的、欺诈性商业行为。ChipSourceTek对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由ChipSourceTek提供, 但他们将独力负责满足与其产品及在其应用中使用ChipSourceTek产品 相关的所有法 律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障 及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何ChipSourceTek组件而对ChipSourceTek及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对ChipSourceTek组件进行特别的促销。ChipSourceTek的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用 的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

ChipSourceTek 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。 只有那些ChipSourceTek特别注明属于军用等级或"增强型塑料"的ChipSourceTek组件才是设计或专门用于军事/航空应用或环境

的。购买者认可并同 意, 对并非指定面 向军事或航空航天用途的ChipSourceTek组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有 法律和法规要求。

ChipSourceTek已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要 求, ChipSourceTek不承担任何责任。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8837DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	837	Samples
DRV8837DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	837	Samples
DRV8838DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 85	838	Samples
DRV8838DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	838	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

深圳市矽源特科技有限公司
ShenZhen ChipSourceTek Technology Co. ,Ltd.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)
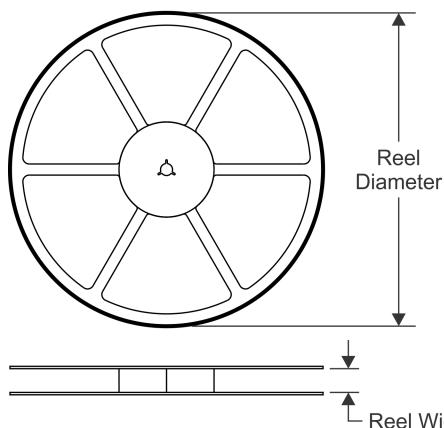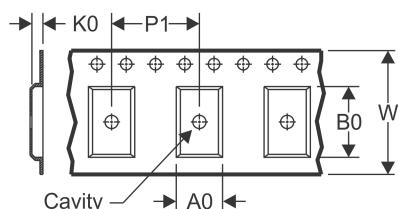
TAPE DIMENSIONS

| A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants
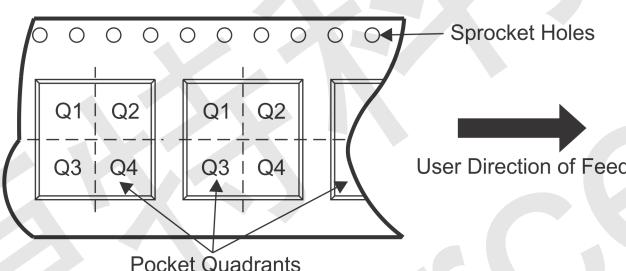
*All dimensions are nominal

| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8838DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS
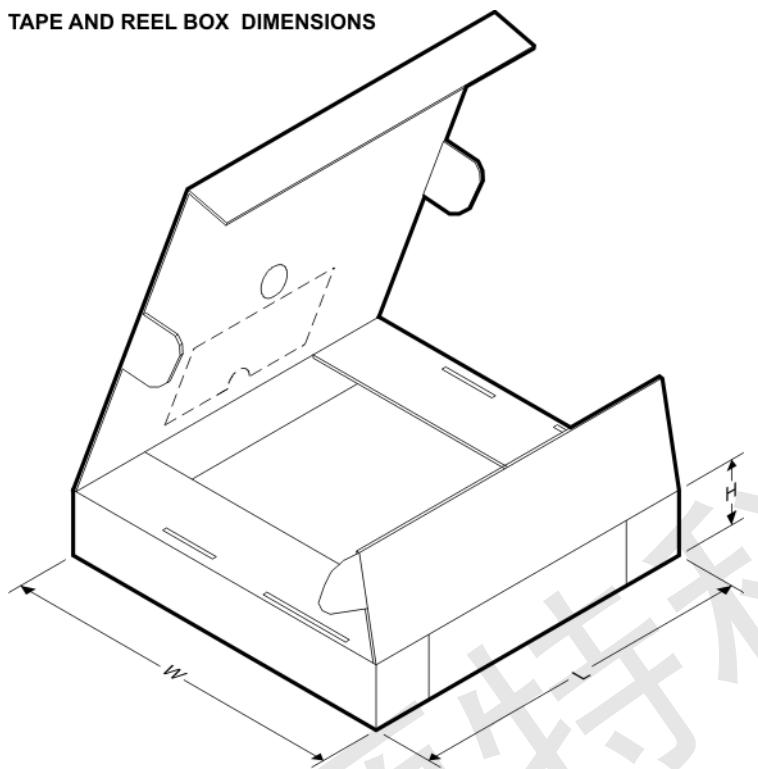
*All dimensions are nominal

| Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8837DSGT	WSON	DSG	8	250	210.0	185.0	35.0
DRV8838DSGT	WSON	DSG	8	250	210.0	185.0	35.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4208210/C

A 2.1 / 1.9 B

PIN 1 INDEX AREA

2.1 / 1.9

0.3 / 0.2

0.4 / 0.2

OPTIONAL TERMINAL
TYPICAL

0.8 MAX

C

SEATING PLANE

0.05 / 0.00

0.08 C

EXPOSED
THERMAL PAD

0.9±0.1

4

5

6X 0.5

2X 1.5

9

1.6±0.1

1

8

SEE OPTIONAL
TERMINAL

PIN 1 ID

8X 0.4 / 0.2

8X 0.3 / 0.2

(0.2) TYP

0.1 M C A B
0.05 M C
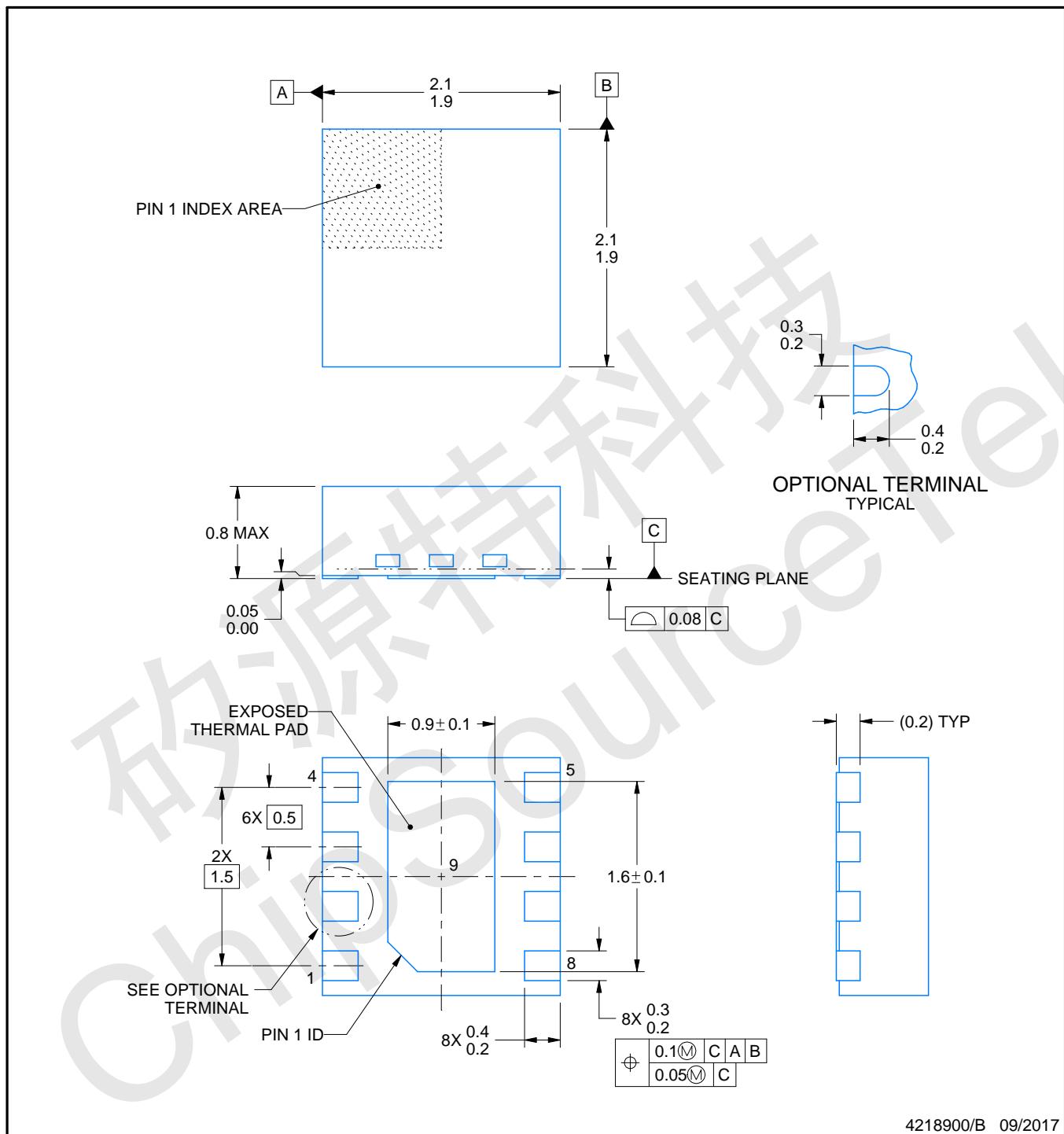
4218900/B 09/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

LAND PATTERN EXAMPLE
SCALE:20X

SOLDER MASK DETAILS

0.07 MAX
ALL AROUND

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED
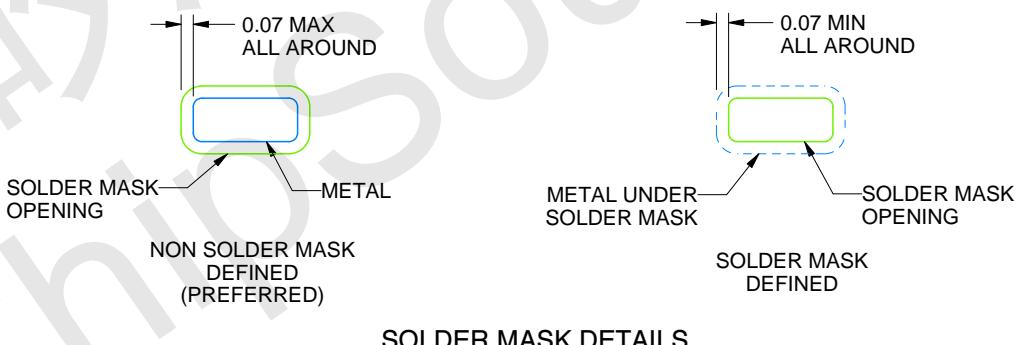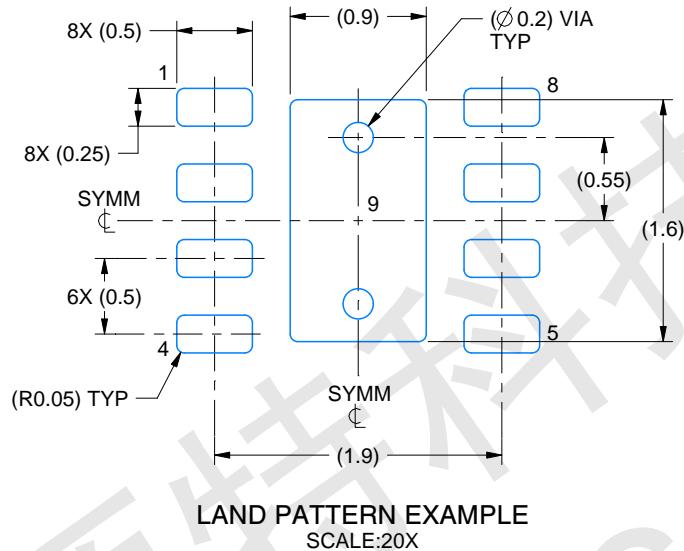
4218900/B   09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
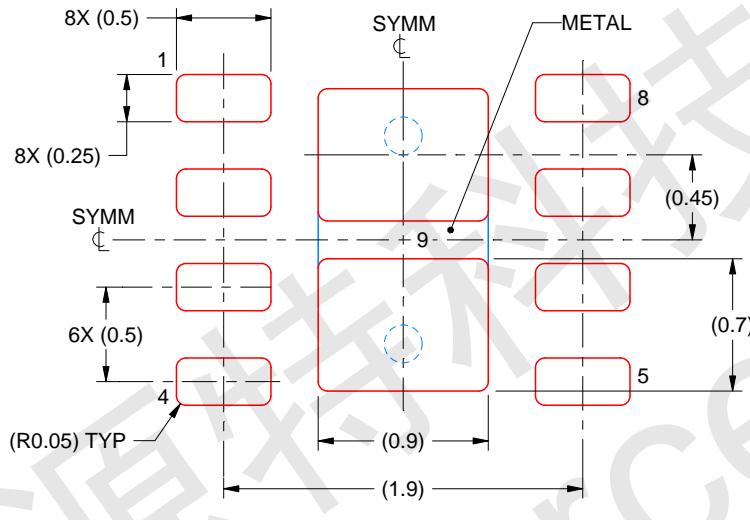
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/B 09/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明

深圳市矽源特科技有限公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的ChipSourceTek销售条款与条件。

ChipSourceTek保证其所销售的组件的性能符合产品销售时 ChipSourceTek半导体产品销售条件与条款的适用规范。仅在ChipSourceTek 保证的范围内，且 ChipSourceTek认为 有必要时才会使 用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

ChipSourceTek对应用帮助或客户产品设计不承担任何义务。客户应对其使用ChipSourceTek组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

ChipSourceTek不对任何ChipSourceTek专利权、版权、屏蔽作品权或其它与使用了ChipSourceTek组件或服务的组合设备、机器或流程相关的ChipSourceTek知识产权中授予 的直接或隐含权 限作出任何保证或解释。ChipSourceTek所发布的与第三方产品或服务有关的信息，不能构成从ChipSourceTek获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是ChipSourceTek的专利权或其它 知识产权方面的许可。

对于ChipSourceTek的产品手册或数据表中ChipSourceTek信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行 复制。ChipSourceTek对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售ChipSourceTek组件或服务时，如果对该组件或服务参数的陈述与ChipSourceTek标明的参数相比存在差异或虚假成分，则会失去相关ChipSourceTek 组件 或服务的所有明 示或暗示授权，且这是不正当的、欺诈性商业行为。ChipSourceTek对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由ChipSourceTek提供，但他们将独力负责满足与其产品及在其应用中使用ChipSourceTek产品 相关的所有法 律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障 及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何ChipSourceTek组件而对ChipSourceTek及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对ChipSourceTek组件进行特别的促销。ChipSourceTek的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用 的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

ChipSourceTek 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。 只有那些ChipSourceTek特别注明属于军用等级或"增强型塑料"的ChipSourceTek组件才是设计或专门用于军事/航空应用或环境

的。购买者认可并同 意，对并非指定面 向军事或航空航天用途的ChipSourceTek组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有 法律和法规要求。

ChipSourceTek已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要 求，ChipSourceTek不承担任何责任。