



N-Channel Enhancement Mode Power MOSFET

Description

The PED645K uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It can be used in a wide variety of applications. It is ESD protected.

General Features

- $V_{DS} = 18V$, $I_D = 10A$

$R_{DS(ON)} < 6.5m\Omega$ @ $V_{GS}=4.5V$

$R_{DS(ON)} < 7m\Omega$ @ $V_{GS}=3.8V$

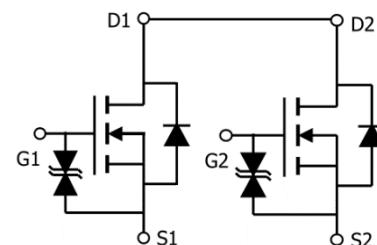
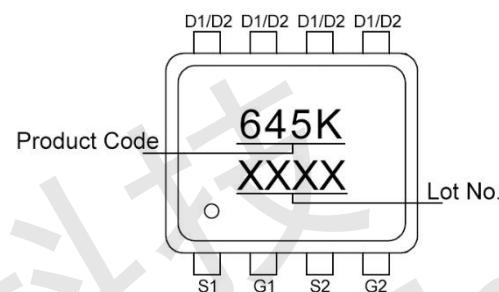
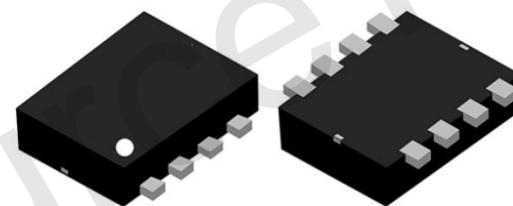
$R_{DS(ON)} < 8.5m\Omega$ @ $V_{GS}=2.5V$

ESD Rating: 2000V HBM

- High Power and current handling capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management
- Battery protection

**Schematic diagram****Marking and pin assignment****DFN3x3-8L****Absolute Maximum Ratings (TA=25°C unless otherwise noted)**

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	18	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	10	A
Drain Current-Continuous (TA=70°C)	I_D	8	A
Pulsed Drain Current (Note 1)	I_{DM}	40	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	62.5	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	V_{DSS}	$V_{GS}=0V, I_D=250\mu A$	18	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=16V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	± 10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.65	1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=6A$	4	5	6.5	$m\Omega$
		$V_{GS}=3.8V, I_D=5.5A$	4.5	5.2	7	$m\Omega$
		$V_{GS}=2.5V, I_D=5.5A$	5	5.9	8.5	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=7A$	-	70	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, F=1.0MHz$	-	1920	-	pF
Output Capacitance	C_{oss}		-	295	-	pF
Reverse Transfer Capacitance (Note 4)	C_{rss}		-	285	-	pF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=1.35\Omega, V_{GS}=5V, R_G=3\Omega$	-	2.5	-	nS
Turn-on Rise Time	t_r		-	7.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	4.5	-	nS
Turn-Off Fall Time	t_f		-	10.8	-	nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=7A, V_{GS}=4.5V$	-	17.5	-	nC
Gate-Source Charge	Q_{gs}		-	4.5	-	nC
Gate-Drain Charge	Q_{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_s=1A$	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to product.



Typical Electrical and Thermal Characteristics

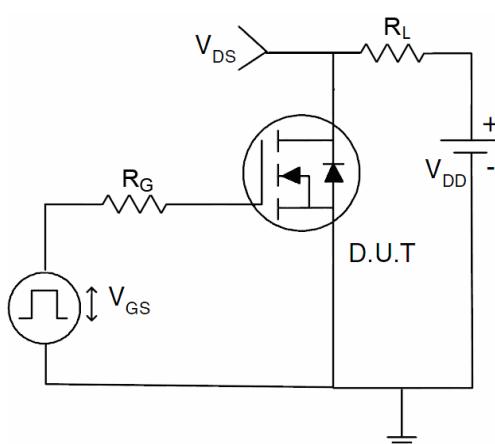


Figure 1 Switching Test Circuit

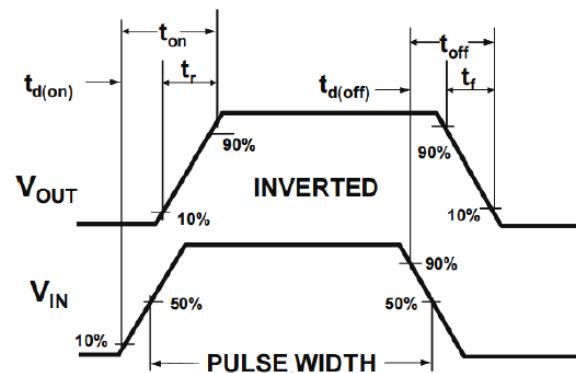
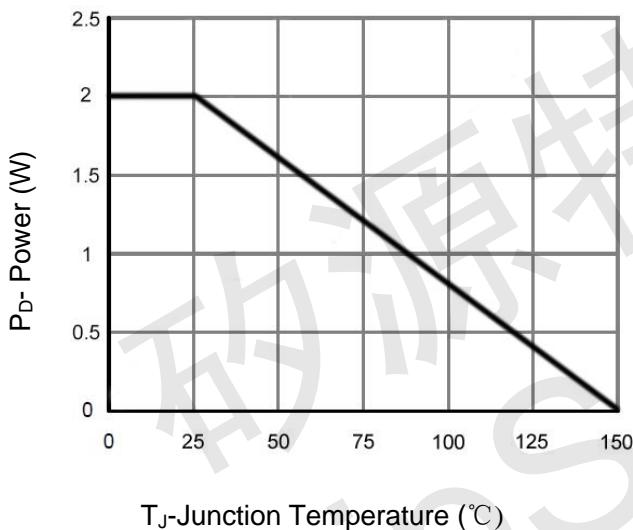
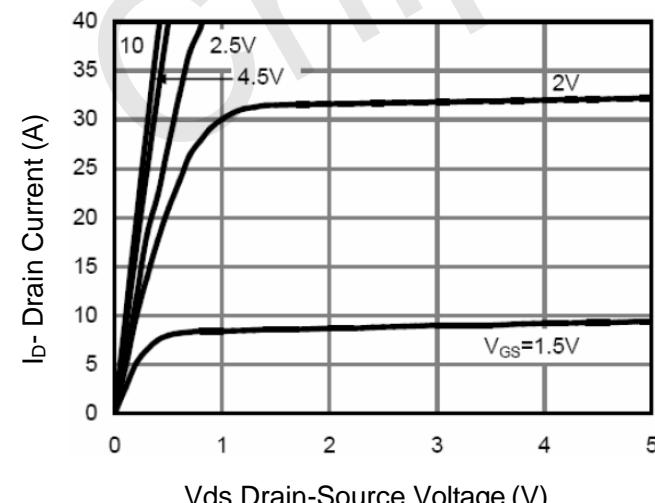


Figure 2 Switching Waveform



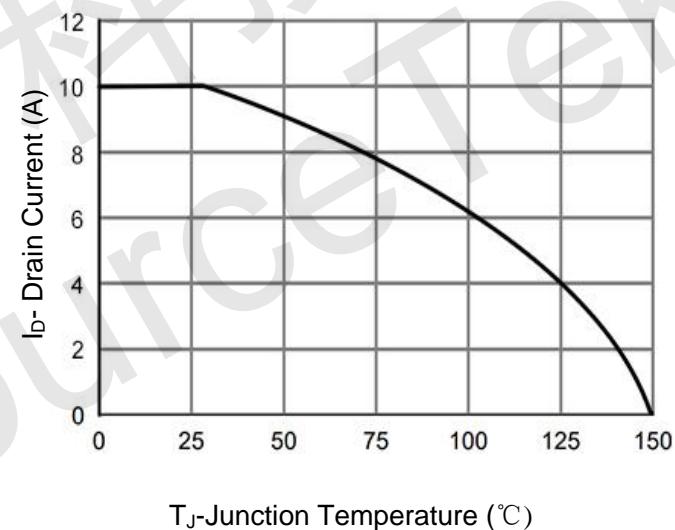
T_J-Junction Temperature (°C)

Figure 3 Power Dissipation



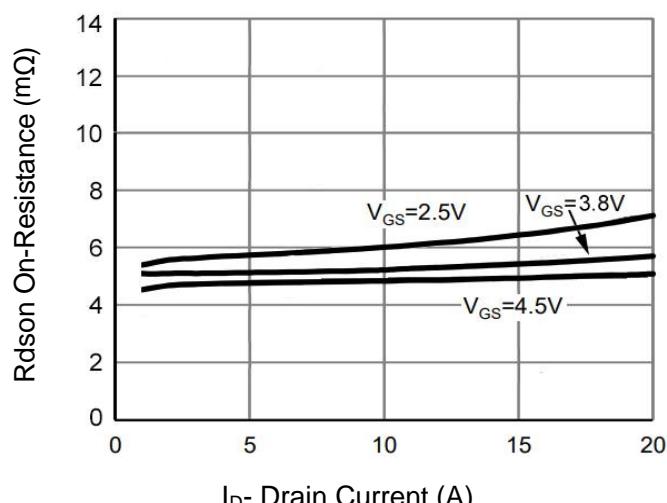
V_{DS} Drain-Source Voltage (V)

Figure 5 Output Characteristics



T_J-Junction Temperature (°C)

Figure 4 Drain Current



I_D- Drain Current (A)

Figure 6 Rdson vs Drain Current

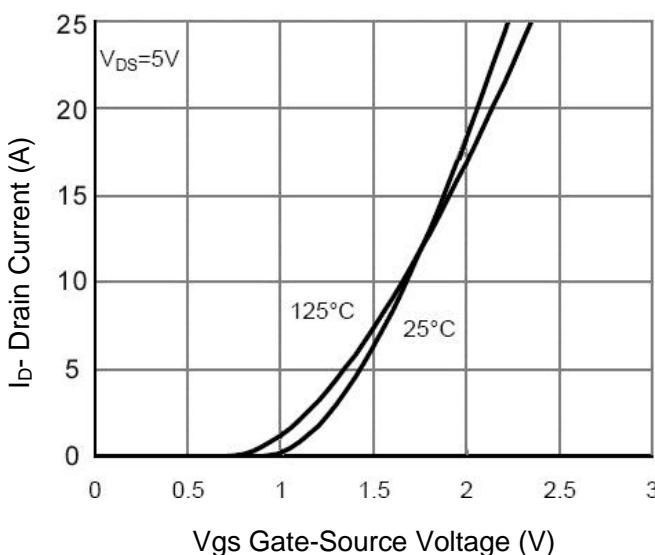


Figure 7 Transfer Characteristics

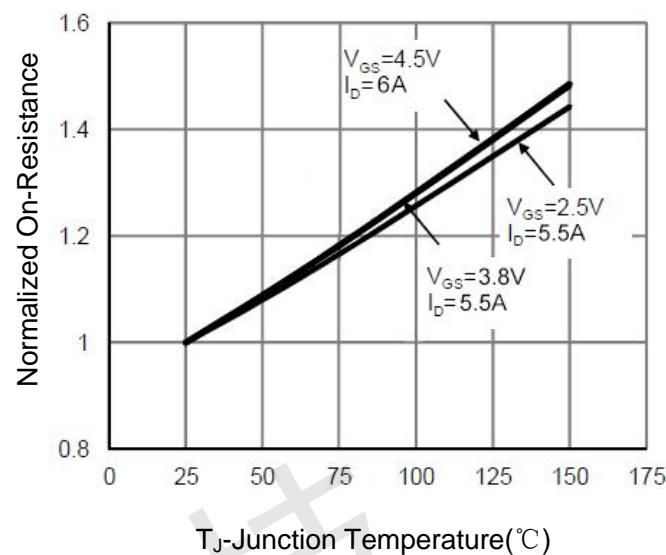


Figure 8 R_{DSON} vs Junction Temperature

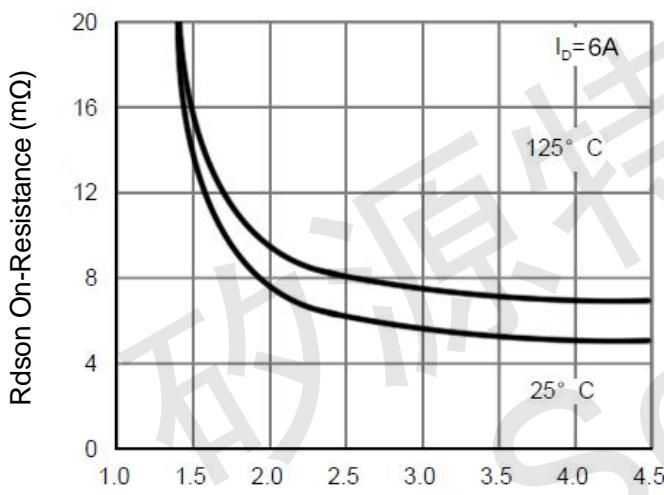


Figure 9 R_{DSON} vs V_{GS}

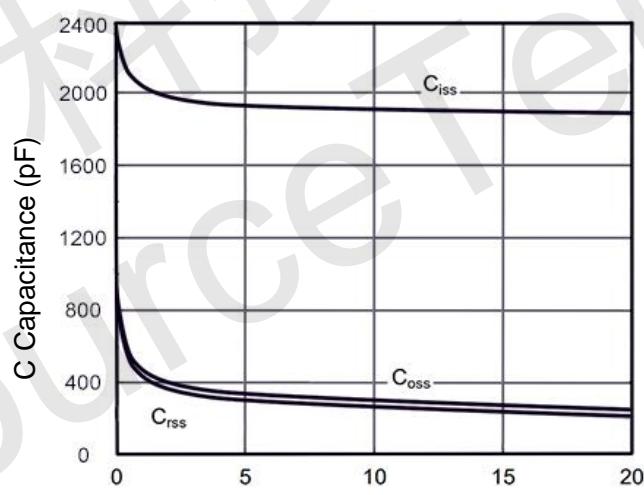


Figure 10 Capacitance vs V_{DS}

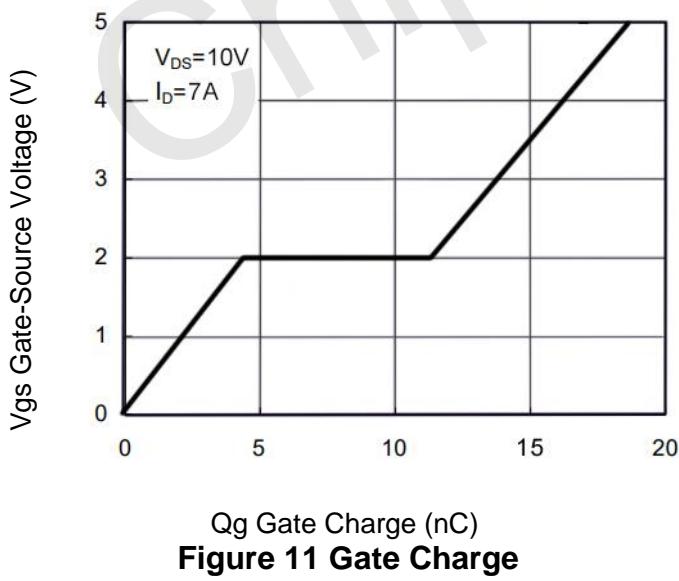


Figure 11 Gate Charge

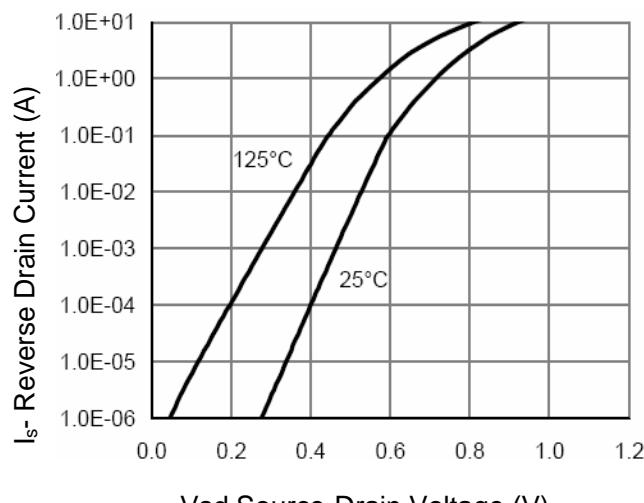


Figure 12 Source-Drain Diode Forward

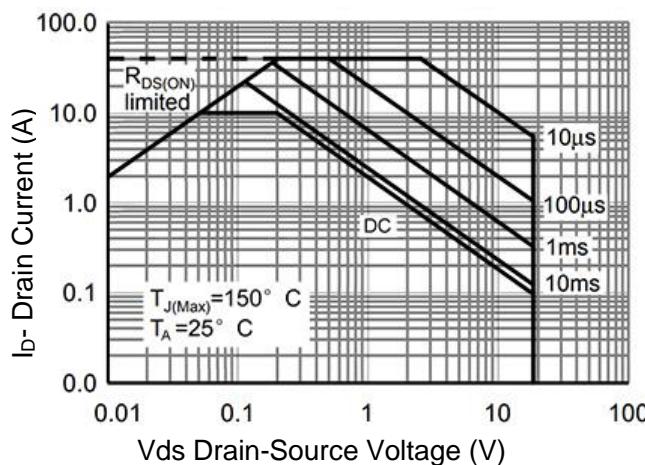


Figure 13 Safe Operation Area

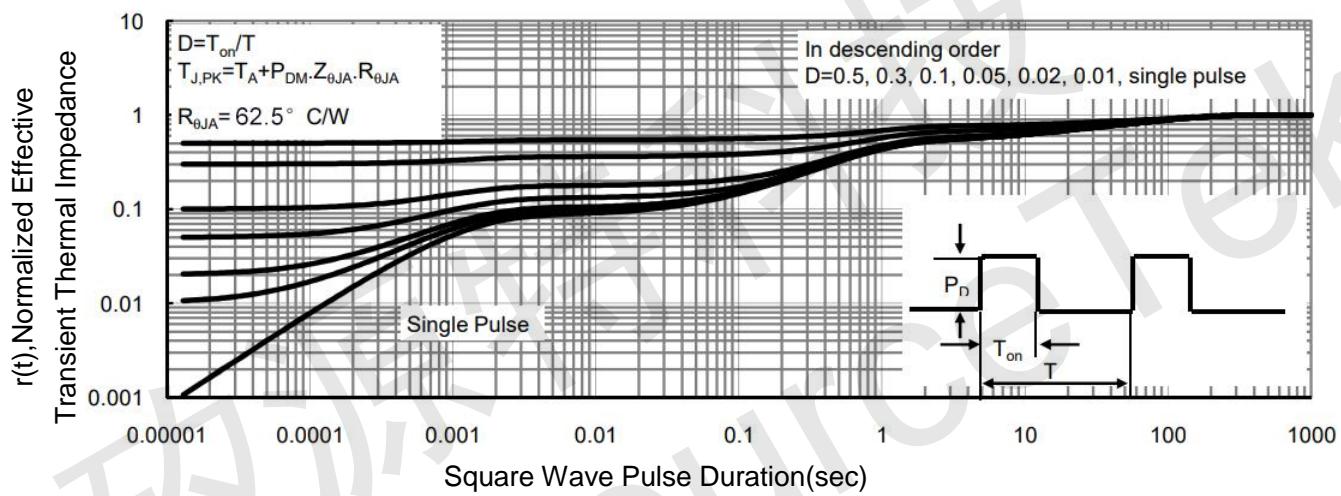
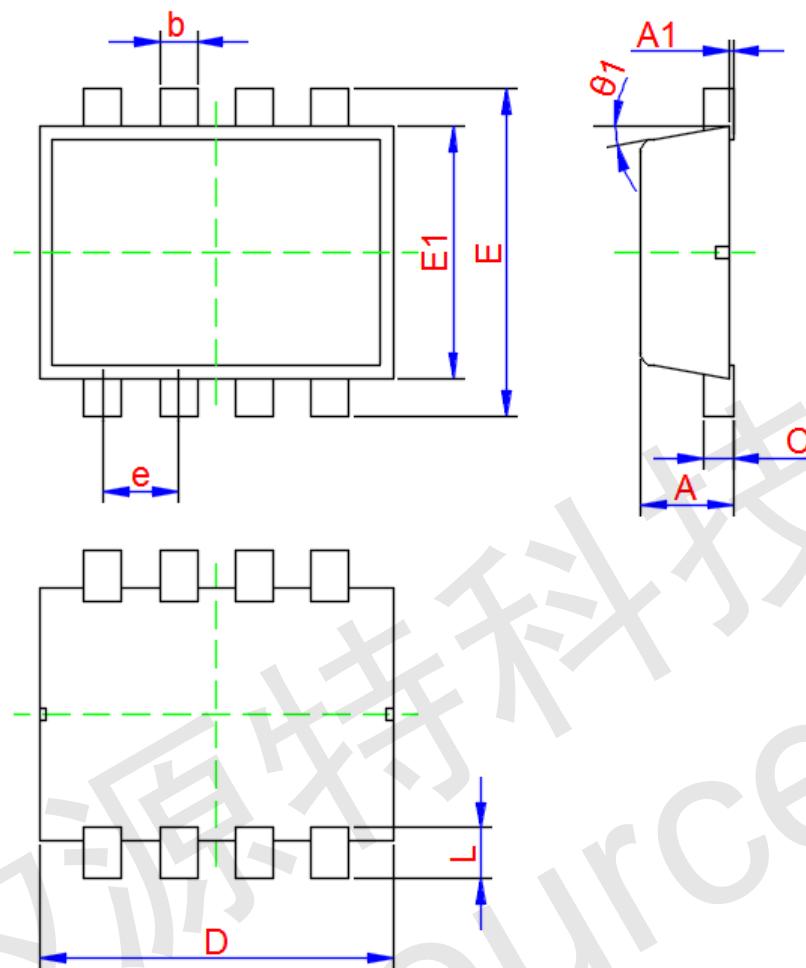


Figure 14 Normalized Maximum Transient Thermal Impedance



DFN3x3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.700	0.800	0.900
A1	0.000	-	0.050
b	0.240	0.300	0.350
c	0.080	0.150	0.250
D	2.800	2.900	3.000
E	2.700	2.800	2.900
E1	2.200	2.300	2.400
e	0.650TYP.		
L	0.200	0.380	0.450
Θ_1	0°	10°	12°