



CSTS60N04F N-Ch 40V Fast Switching MOSFETs

CSTS60N04F Features

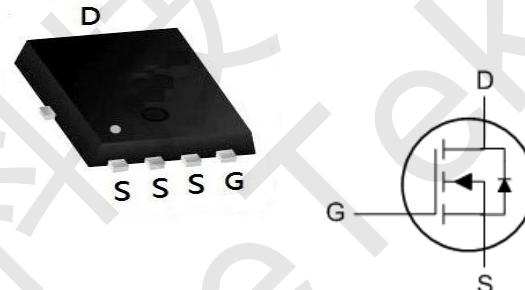
- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

CSTS60N04F Product Summary



BVDSS	RDS(on)	ID
40V	6.9mΩ	60A

CSTS60N04F PDFN5060-8L Pin Configuration



CSTS60N04F Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current ¹	60	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current ¹	35	A
I_{DM}	Pulsed Drain Current ²	130	A
EAS	Single Pulse Avalanche Energy ³	48	mJ
I_{AS}	Avalanche Current	35	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	39	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

CSTS60N04F Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	---	60	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.2	°C/W



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CSTS60N04F Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_D=250\mu\text{A}$	40	---	---	V
$\text{R}_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$\text{V}_{\text{GS}}=10\text{V}$, $\text{I}_D=12\text{A}$	---	6.9	8.5	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}$, $\text{I}_D=10\text{A}$	---	10.0	15	
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{GS}}=\text{V}_{\text{DS}}$, $\text{I}_D=250\mu\text{A}$	1.35	---	3	V
I_{DSS}	Drain-Source Leakage Current	$\text{V}_{\text{DS}}=32\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $\text{T}_J=25^{\circ}\text{C}$	---	---	1	uA
		$\text{V}_{\text{DS}}=32\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $\text{T}_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$\text{V}_{\text{GS}}=\pm 20\text{V}$, $\text{V}_{\text{DS}}=0\text{V}$	---	---	± 100	nA
R_g	Gate Resistance	$\text{V}_{\text{DS}}=0\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$\text{V}_{\text{DS}}=20\text{V}$, $\text{V}_{\text{GS}}=4.5\text{V}$, $\text{I}_D=12\text{A}$	---	5.8	---	nC
Q_{gs}	Gate-Source Charge		---	3	---	
Q_{gd}	Gate-Drain Charge		---	1.2	---	
$\text{T}_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}}=15\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{R}_G=3.3\Omega$	---	14.3	---	ns
T_r	Rise Time		---	5.6	---	
$\text{T}_{\text{d(off)}}$	Turn-Off Delay Time		---	20	---	
T_f	Fall Time		---	11	---	
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=15\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	690	---	pF
C_{oss}	Output Capacitance		---	193	---	
C_{rss}	Reverse Transfer Capacitance		---	38	---	

CSTS60N04F Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,5}	$\text{V}_G=\text{V}_D=0\text{V}$, Force Current	---	---	60	A
V_{SD}	Diode Forward Voltage ²	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_s=1\text{A}$, $\text{T}_J=25^{\circ}\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $\text{V}_{\text{DD}}=25\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{L}=0.1\text{mH}$, $\text{I}_{\text{AS}}=31\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



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CSTS60N04F Typical Characteristics

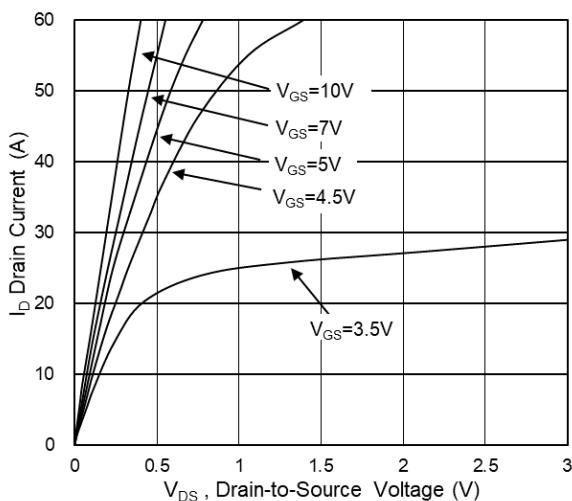


Fig.1 Typical Output Characteristics

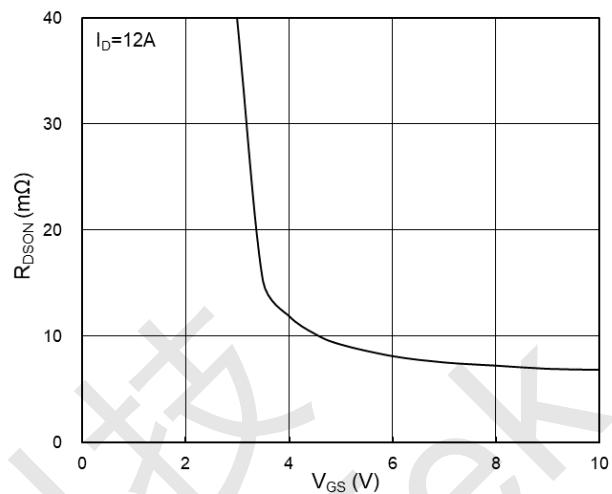


Fig.2 On-Resistance vs G-S Voltage

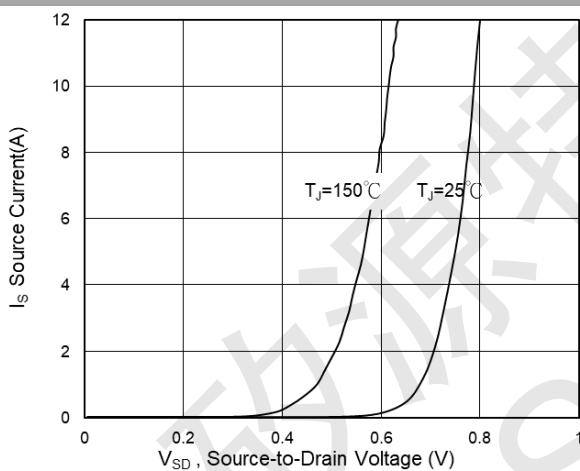


Fig.3 Source Drain Forward Characteristics

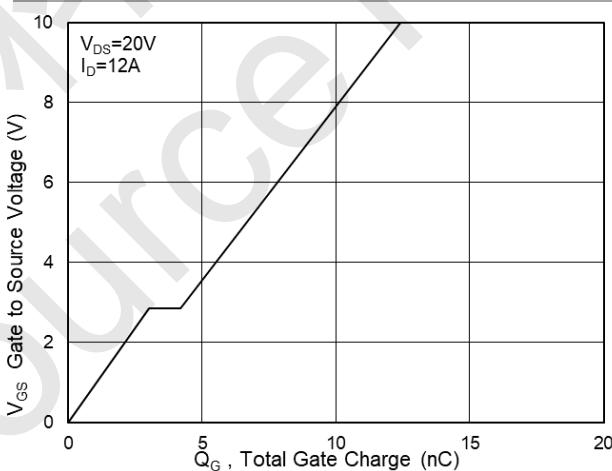


Fig.4 Gate-Charge Characteristics

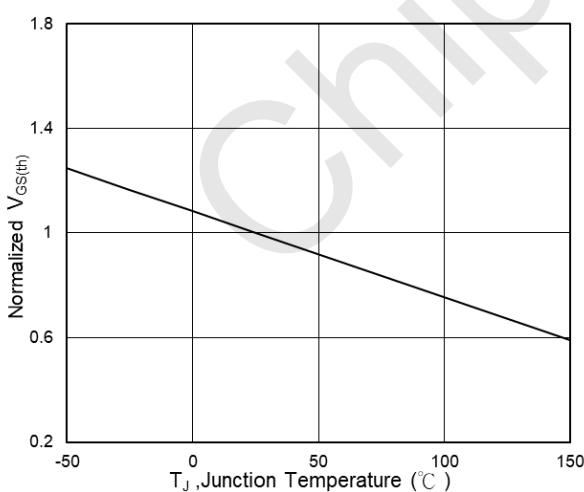


Fig.5 Normalized $V_{GS(th)}$ vs T_J

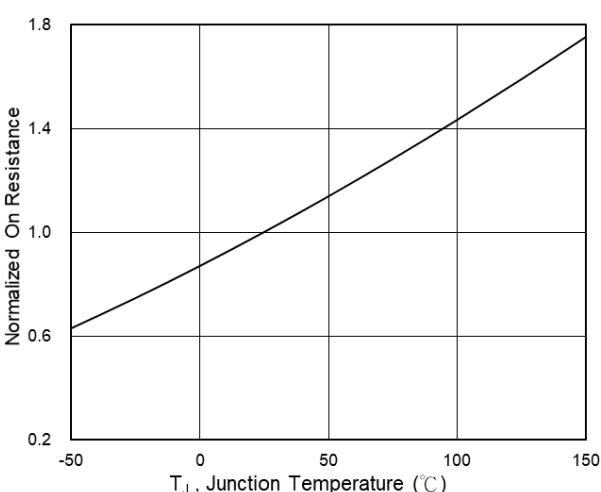


Fig.6 Normalized $R_{DS(on)}$ vs T_J



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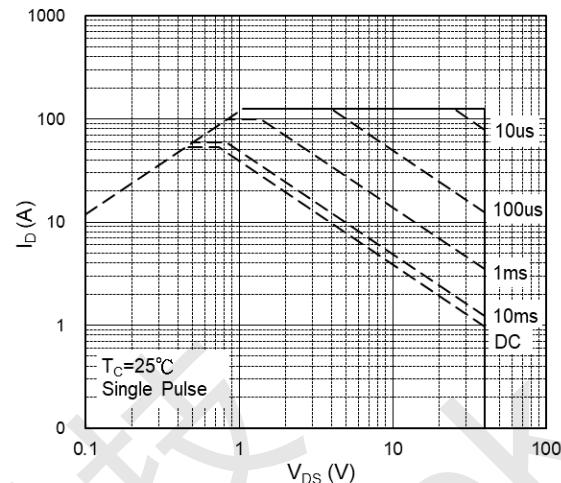
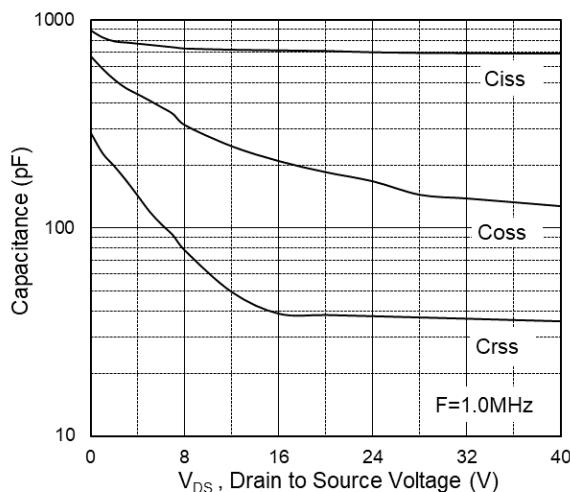


Fig.7 Capacitance

Fig.8 Safe Operating Area

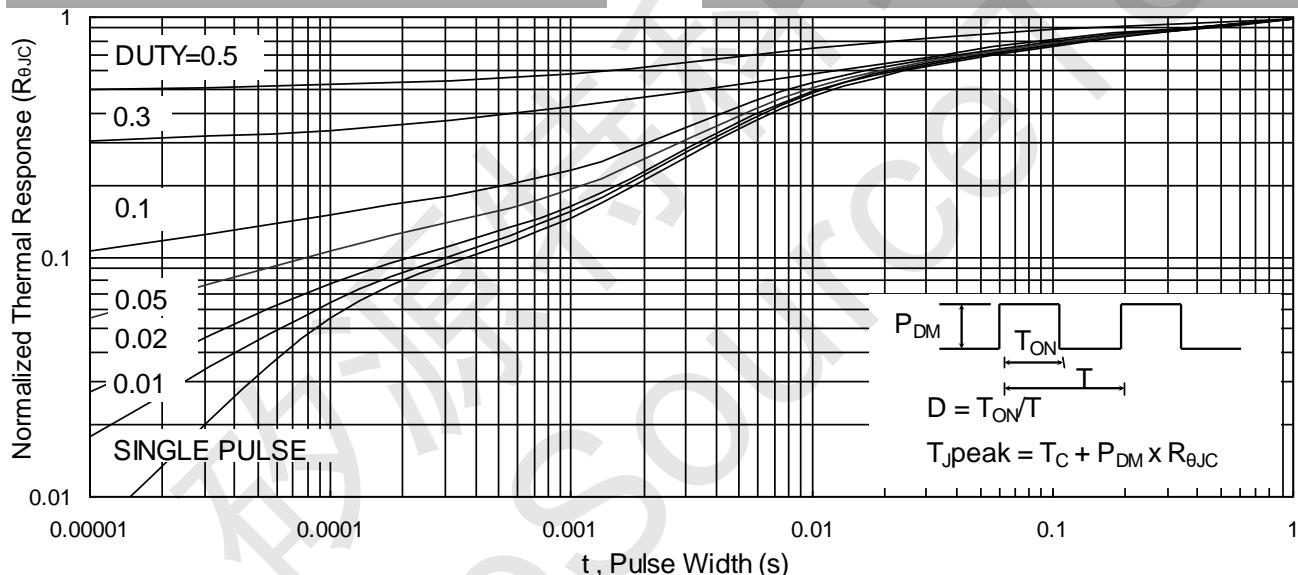


Fig.9 Normalized Maximum Transient Thermal Impedance

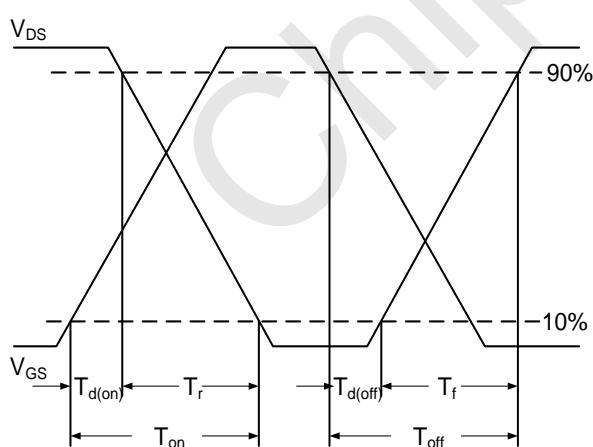


Fig.10 Switching Time Waveform

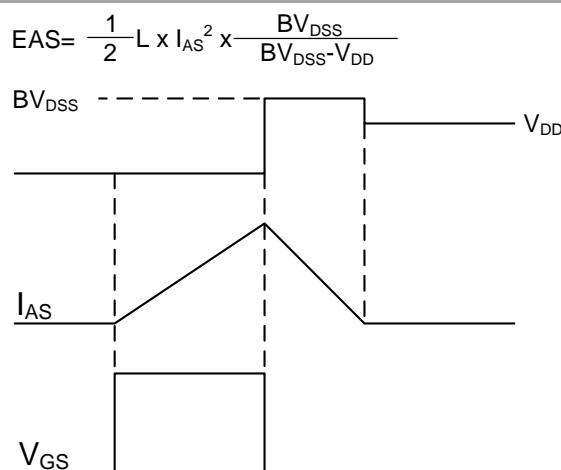
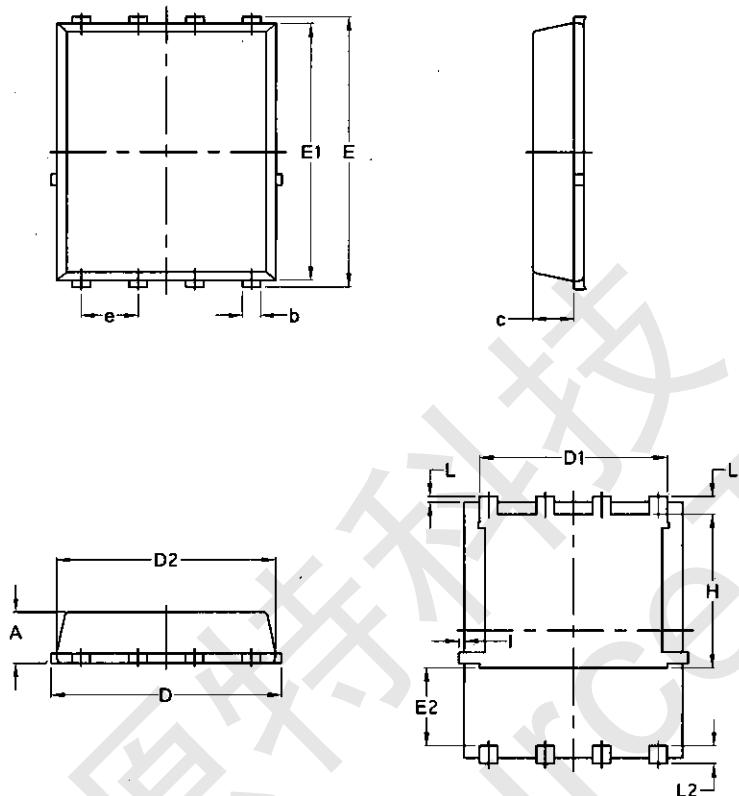


Fig.11 Unclamped Inductive Waveform



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CSTS60N04F Package Mechanical Data-PDFN5060-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070