



CSTS4896D Dual N-Ch 40V Fast Switching MOSFETs

CSTS4896D Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

CSTS4896D Applications

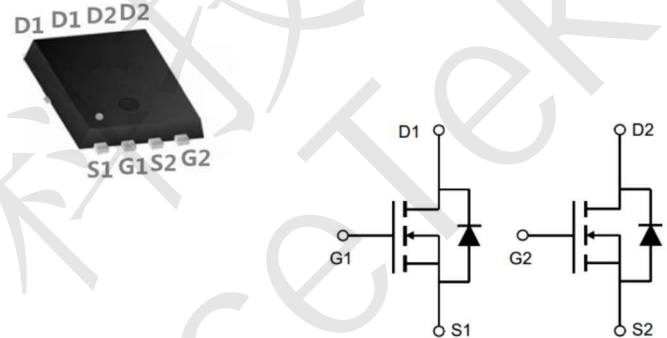
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

CSTS4896D Product Summary



BVDSS	R _{DS(ON)}	ID
40V	7.2mΩ	40A

CSTS4896D PDFN3333-8L Pin Configuration



CSTS4896D Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	40	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	20	A
I_{DM}	Pulsed Drain Current ²	180	A
EAS	Single Pulse Avalanche Energy ³	26.1	mJ
I_{AS}	Avalanche Current	15	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	43.6	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

CSTS4896D Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2.8	$^\circ C/W$



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CSTS4896D Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=12A$	---	7.2	9.5	m Ω
		$V_{GS}=4.5V, I_D=10A$	---	10.0	15	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.35	---	3	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=12A$	---	5.8	---	nC
Q_{gs}	Gate-Source Charge		---	3	---	
Q_{gd}	Gate-Drain Charge		---	1.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=1A$	---	14.3	---	ns
T_r	Rise Time		---	5.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	20	---	
T_f	Fall Time		---	11	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	690	---	pF
C_{oss}	Output Capacitance		---	193	---	
C_{rSS}	Reverse Transfer Capacitance		---	38	---	

CSTS4896D Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	40	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=31A$
4. The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



CSTS4896D Typical Characteristics

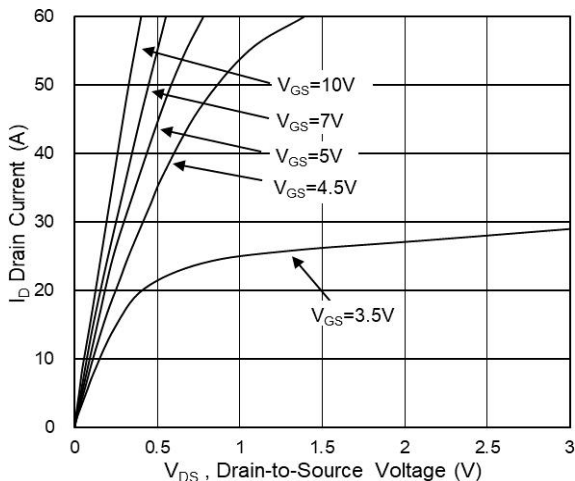


Fig.1 Typical Output Characteristics

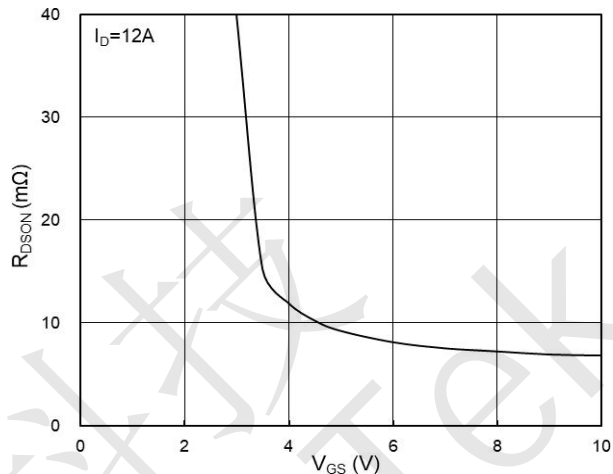


Fig.2 On-Resistance vs G-S Voltage

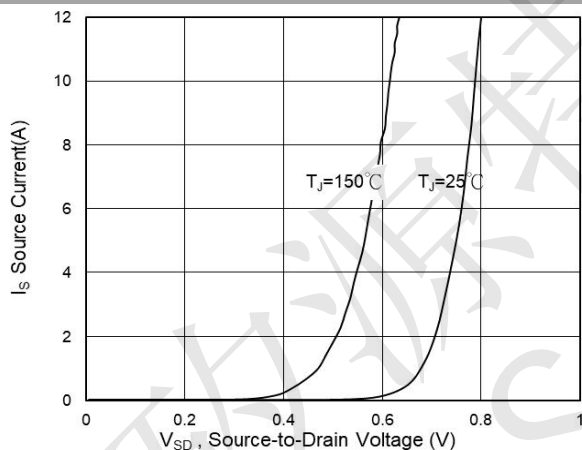


Fig.3 Source Drain Forward Characteristics

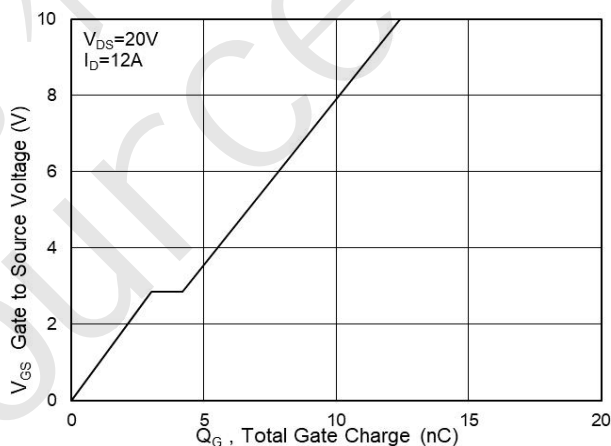


Fig.4 Gate-Charge Characteristics

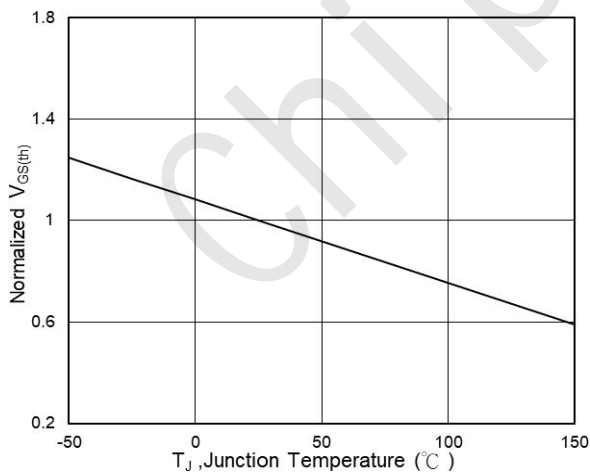


Fig.5 Normalized $V_{GS(th)}$ vs T_J

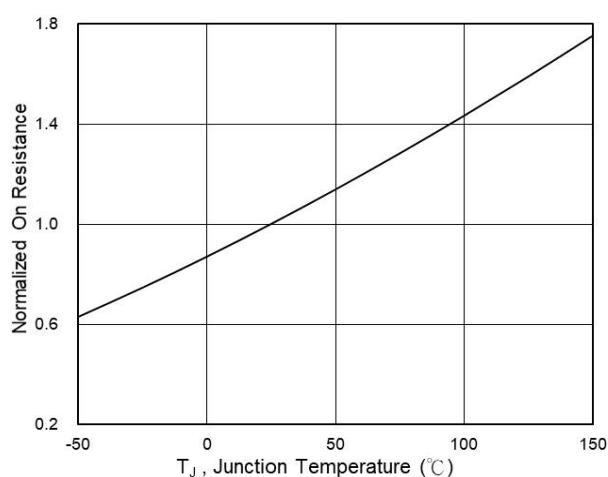


Fig.6 Normalized $R_{DS(on)}$ vs T_J



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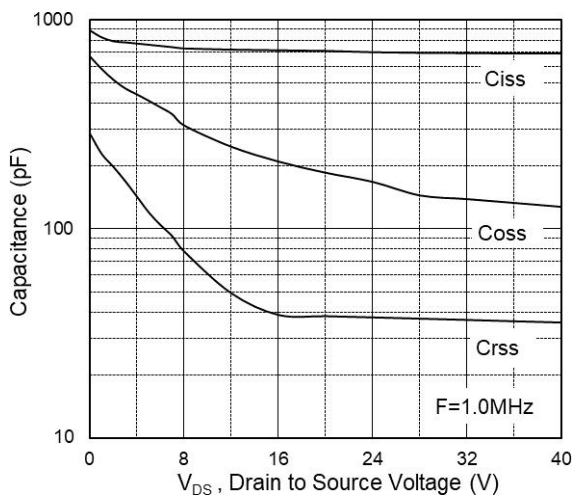


Fig.7 Capacitance

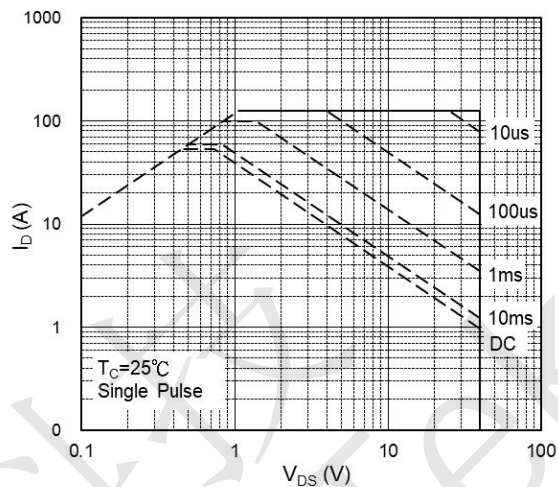


Fig.8 Safe Operating Area

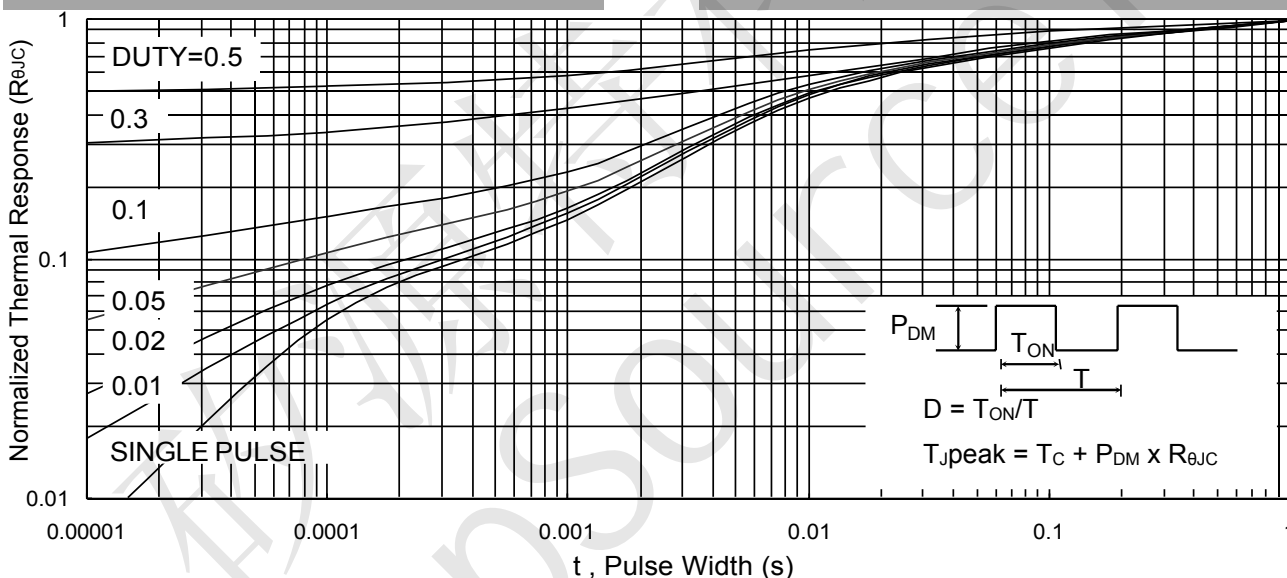
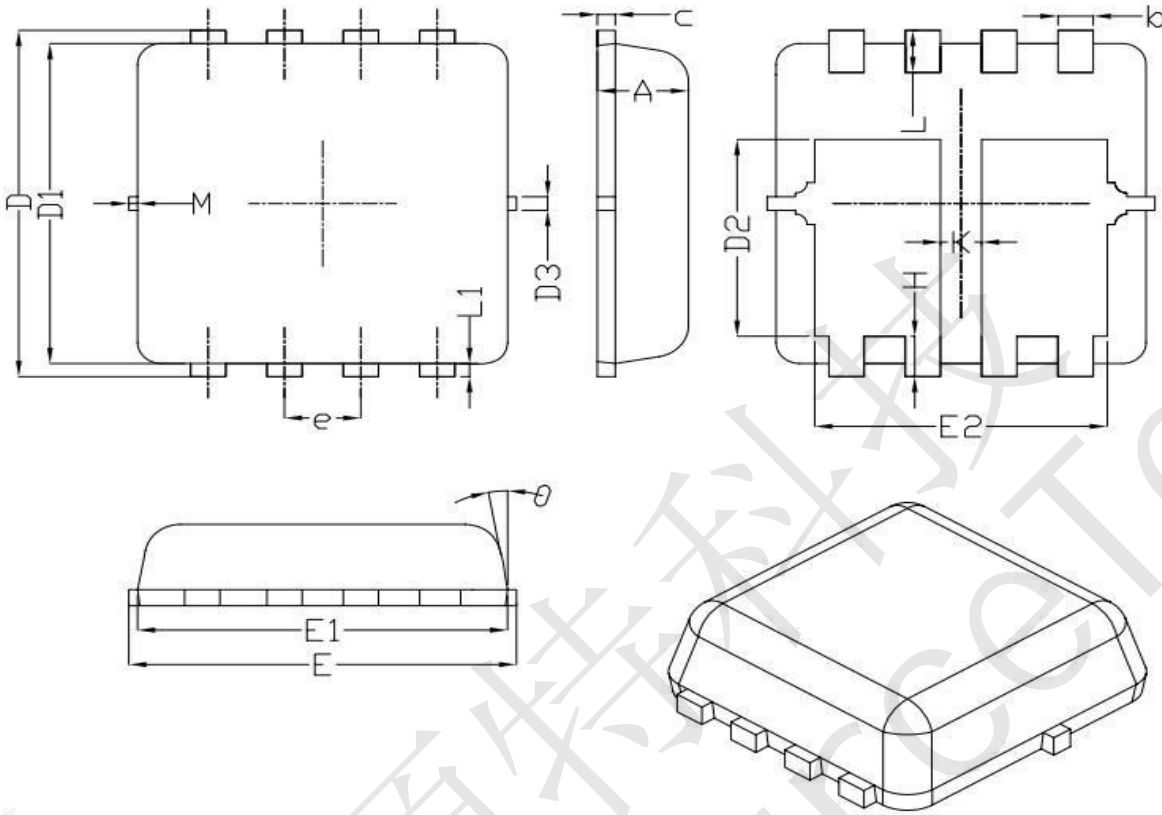


Fig.9 Normalized Maximum Transient Thermal Impedance



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CSTS4896D Dual PDFN3X 3 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.