CSTS40N10 N-Ch 100V Fast Switching MOSFETs

CSTS40N10 Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

CSTS40N10 Product Summary

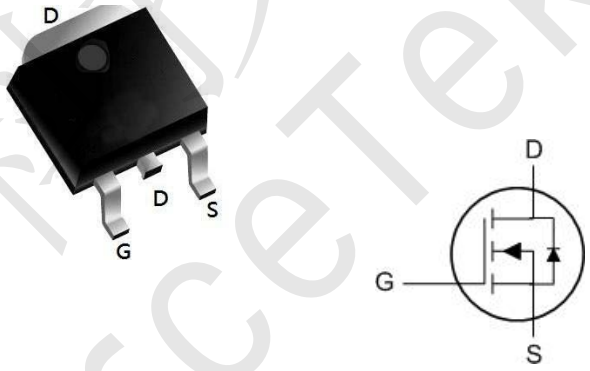
Green

BVDSS	RDSON	ID
100V	20 mΩ	40A

CSTS40N10 Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

CSTS40N10 TO252 Pin Configuration



CSTS40N10 Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current note5	T_C = 25℃	40	A
I_D	Continuous Drain Current note5	T_C = 100℃	16	A
I_{DM}	Pulsed Drain Current note3		100	A
P_D	Power Dissipation note2	T_C = 25℃	27	W
I_{AS}	Avalanche Current note3,6		8	A
E_{AS}	Single Pulse Avalanche Energy note3,6		16	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case		4.65	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient note1,4		62	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

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CSTS40N10 Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.6	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 15A	-	20	23	mΩ
		V_{GS} = 4.5V, I_D = 10A	-	-	33	mΩ
g_{fs}	Forward Threshold Voltage	V_{DS}= 10V, I_D= 20A	-	22	-	S
R_g	Gate Resistance	V_{DS} = V_{GS}=0V, f = 1.0MHz	-	1.62	-	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz	-	822	-	pF
C_{oss}	Output Capacitance		-	310	-	pF
C_{rss}	Reverse Transfer Capacitance		-	23.5	-	pF
Switching Characteristics						
Q_g	Total Gate Charge	V_{DS}= 50V, I_D = 20A, V_{GS} = 10V	-	22.7	-	nC
Q_{gs}	Gate-Source Charge		-	6.2	-	
Q_{gd}	Gate-Drain(“Miller”) Charge		-	5.3	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 50V, I_D = 20A, R_G = 3Ω, V_{GS}=10V	-	15	-	ns
t_r	Turn-On Rise Time		-	3.2	-	
$t_{d(off)}$	Turn-Off Delay Time		-	30	-	
t_f	Turn-Off Fall Time		-	7.6	-	
Diode Characteristics						
I_S	Continuous Source Current		-	-	40	A
V_{SD}	Diode Forward Voltage	I_S=20A . V_{GS} = 0V	-	0.88	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD}=20A, dI$_{SD}$/dt=100A/μs	-	45	-	ns
Q_{rr}	Reverse Recovery Charge		-	59	-	nC

Notes:

1. The value of $R_{\theta JC}$ is measured in a still air environment with TA =25°C and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
5. The maximum current rating is package limited.
6. The EAS data shows Max. rating. The test condition is V_{DS}=50V,V_{GS}=10V,L=0.5mH

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CSTS40N10 Typical Performance Characteristics

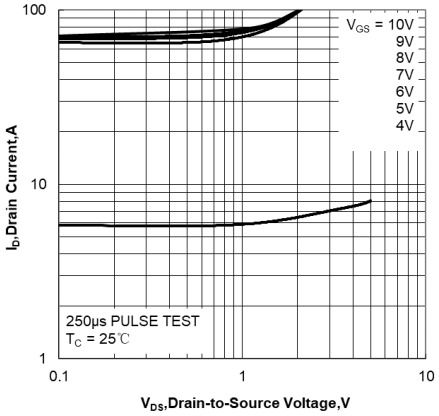

Figure 1. Output Characteristics

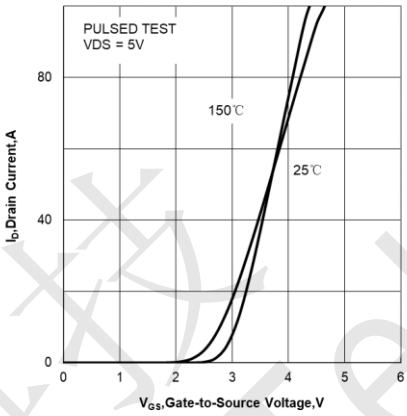

Figure 2. Transfer Characteristics

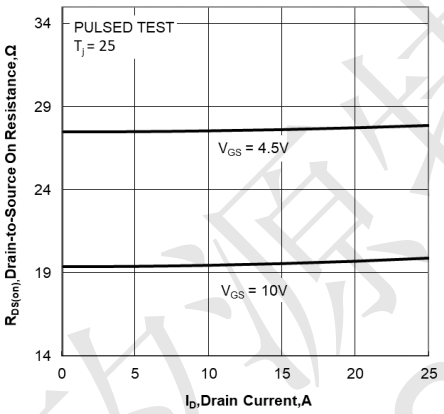

Figure 3. Drain-to-Source On Resistance vs Drain Current

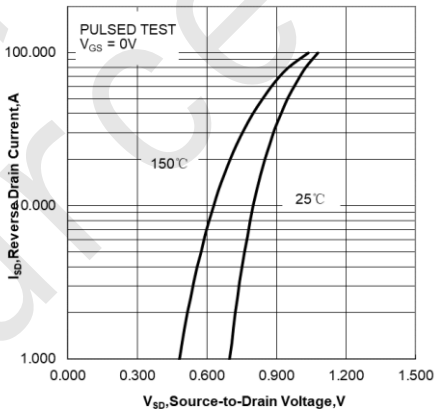

Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

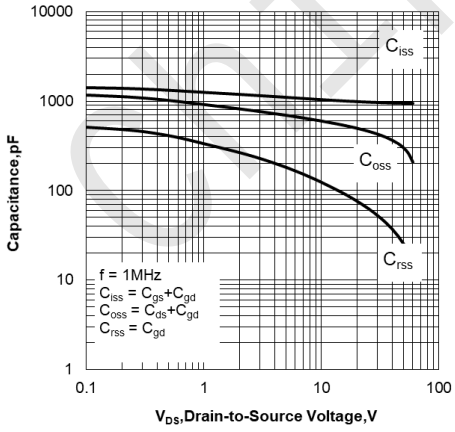

Figure 5. Capacitance Characteristics

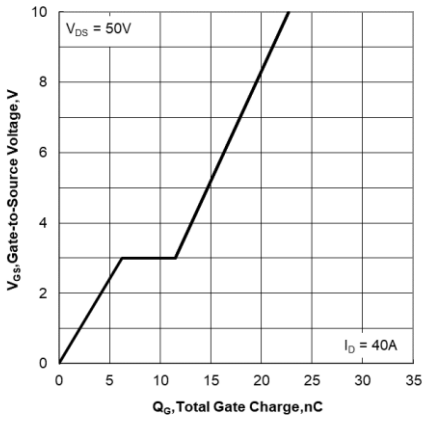

Figure 6. Gate Charge Characteristics

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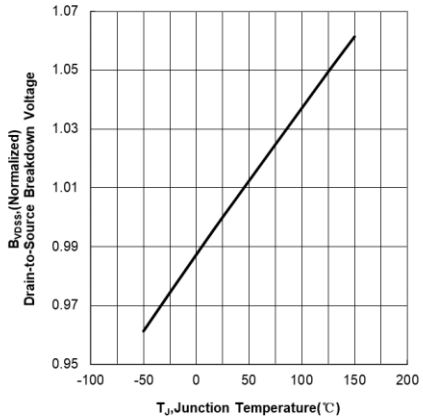


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

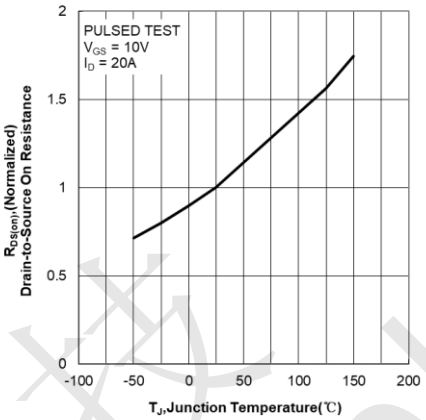


Figure 8. Normalized On Resistance vs Junction Temperature

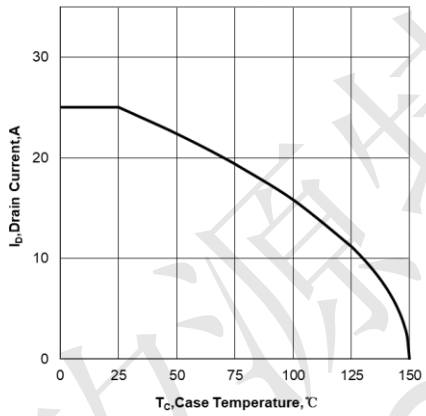


Figure 9. Maximum Continuous Drain Current vs Case Temperature

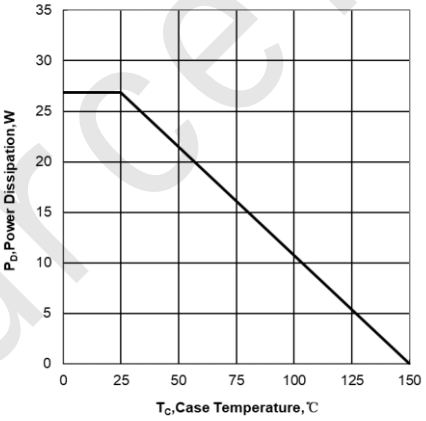


Figure 10. Maximum Power Dissipation vs Case Temperature

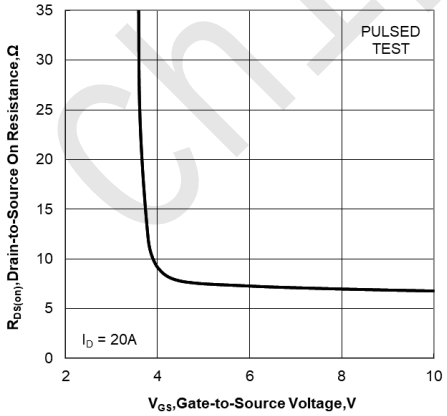


Figure11. Drain-to-Source On Resistance vs Gate

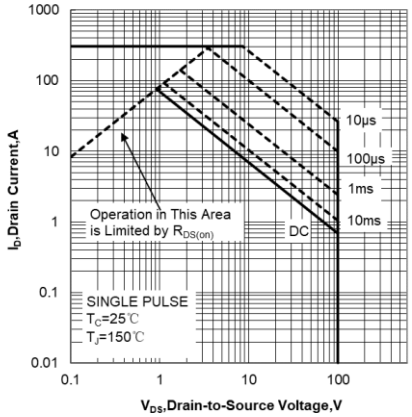


Figure 12. Maximum Safe Operating Area

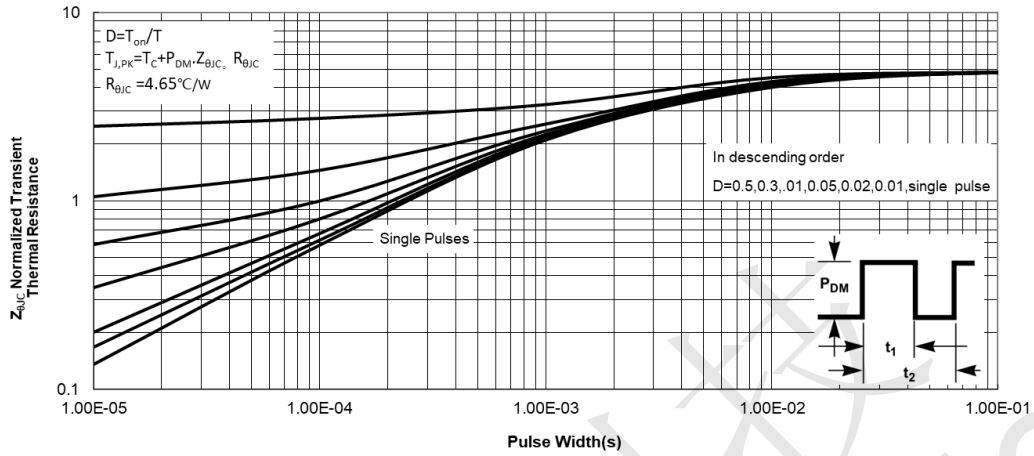
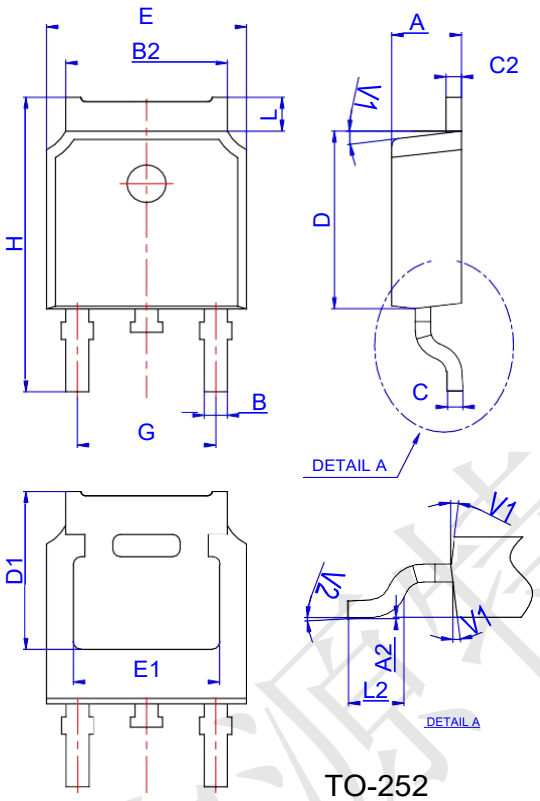


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

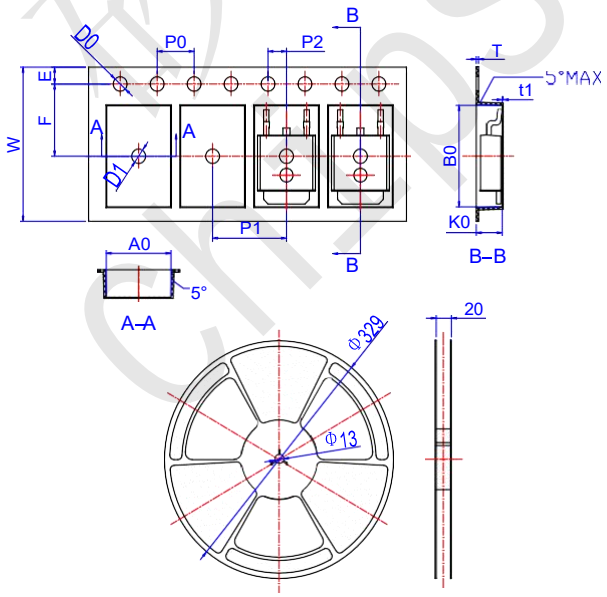
CSTS40N10 Package Mechanical Data TO-252



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

CSTS40N10 Reel Spectification-TO-252-4R



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

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