深圳市矽源特科技有限公司
ShenZhen ChipSoureTek Technology Co.,Ltd.

CST5020D   16-bit constant current LED driver IC

I. CST5020D Product Overview

CST5020D is a driver IC for LED display panel design. Its built-in CMOS shift buffer and latch function can convert serial input data into parallel output data format. The input voltage range of CST5020D is 3.3 V~5V, providing 16 current sources, which can provide 3~36mA constant current in each output stage to drive LED; The current difference of the output channel in a single IC is less than ±2%@I_{OUT} =23.8mA; ±2.5%@I_{OUT} =3mA; the output current difference between multiple ICs is less than ±3%; The current varies with the output withstand voltage (V_{DS}) and is controlled at 0.1% per volt; The current is also controlled to 1% depending on the supply voltage (V_{DD}) and the ambient temperature. The user can adjust the current of each output stage of the CST5020D by selecting external resistors with different resistance values. With this mechanism, the user can accurately control the brightness of the LED.

The CST5020D guarantees an output stage withstand voltage of 11V, so it is possible to connect multiple LEDs in series at each output. In addition, the CST5020D also provides a highclock rate input of 25 MHz to meet the high datatransmissionrequirements of the system.

II. CST5020D Characteristics

➢ 16 constant current output channels;

➢ Constant output value is not affected by the load voltage at the output. Constant current range value:
  3~36mA@V_{DD}=5V;
  3~20mA@V_{DD}=3.3V;

➢ Extremely accurate current output:
  Maximum difference between channels:< ±1.5%(general value) ;< ±2.0%(maximum value)
  Maximum difference between chips:< ±1.5%(general value) ;< ±3.0%(maximum value)

➢ Fast output current control response: minimum pulse width = 35ns (under the condition of maintaining output consistency);

➢ Using an external resistor, the current output value of 16 drive ports can be set;

➢ Schmitt trigger input characteristic;

➢ High data rate up to 25MHz;

➢ Operating voltage range: 3.3V to 5V;

➢ Very low standby current and operating current (i.e. VDD current);

➢ integrate output channel overshoot suppression circuit

➢ Available in SSOP-24 package (wide body: e=1.0mm; narrow body: e=0.635mm)

➢ Used in LED display, variable signs, LED traffic signal indication;

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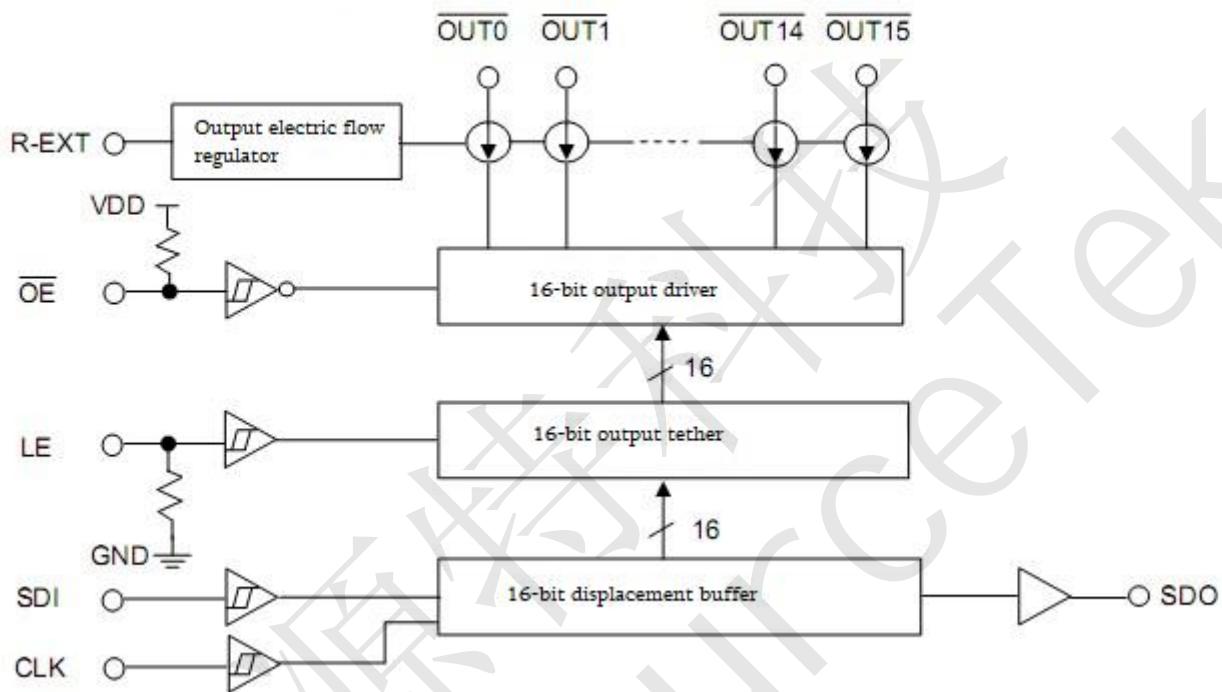
III. CST5020D Pin map and pin description

GND	1		24	V DD
SDI	2		23	REXT
CLK	3		22	SDO
LE	4		21	OE/
OUT0	5		20	OUT15
OUT1	6	CST5020D	19	OUT14
OUT2	7		18	OUT13
OUT3	8		17	OUT12
OUT4	9		16	OUT11
OUT5	10		15	OUT10
OUT6	11		14	OUT9
OUT7	12		13	OUT8

| serial number	Name	Function description
1	GND	Ground terminal for control logic and drive current
2	SDI	input to that serial data input terminal of the shift register.
3	CLK	Clock signal input, data shift is only valid on the rising edge of the clock.
4	LE	Data strobe input. When LE is high, the serial data is passed to the output latch. When LE is low, the data is latched.
5~20	OUT[0:15]	Constant current drive output.
21	OE/	The output enable signal control terminal, OE/, enables the output of OUT0-OUT15 when it is low.
22	SDO	Serial data output for connection to the next driver chip CST5020D.
23	REXT	External resistors set the drive current for all output channels
24	VDD	Positive power supply input.

IV. CST5020D Functional Block Diagram
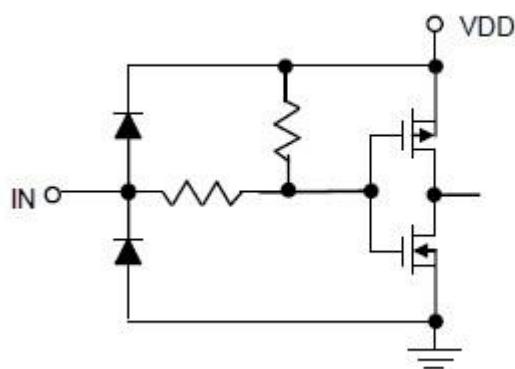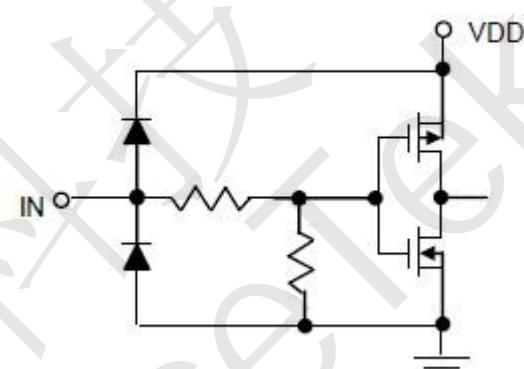
## V. CST5020D Input and output equivalent circuits...
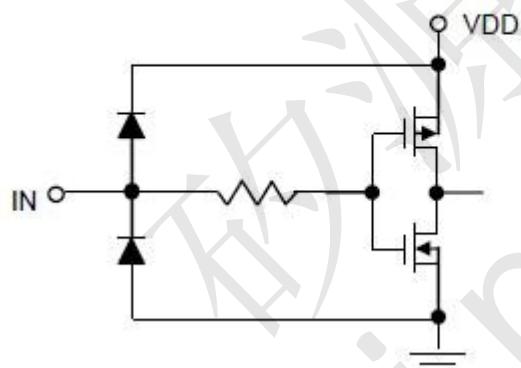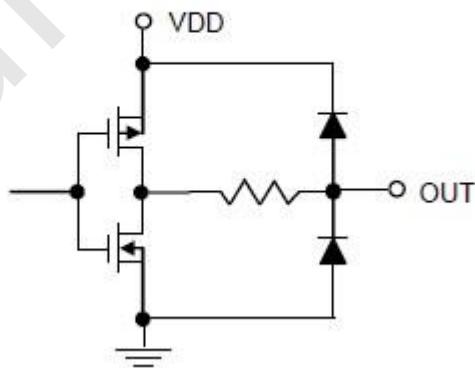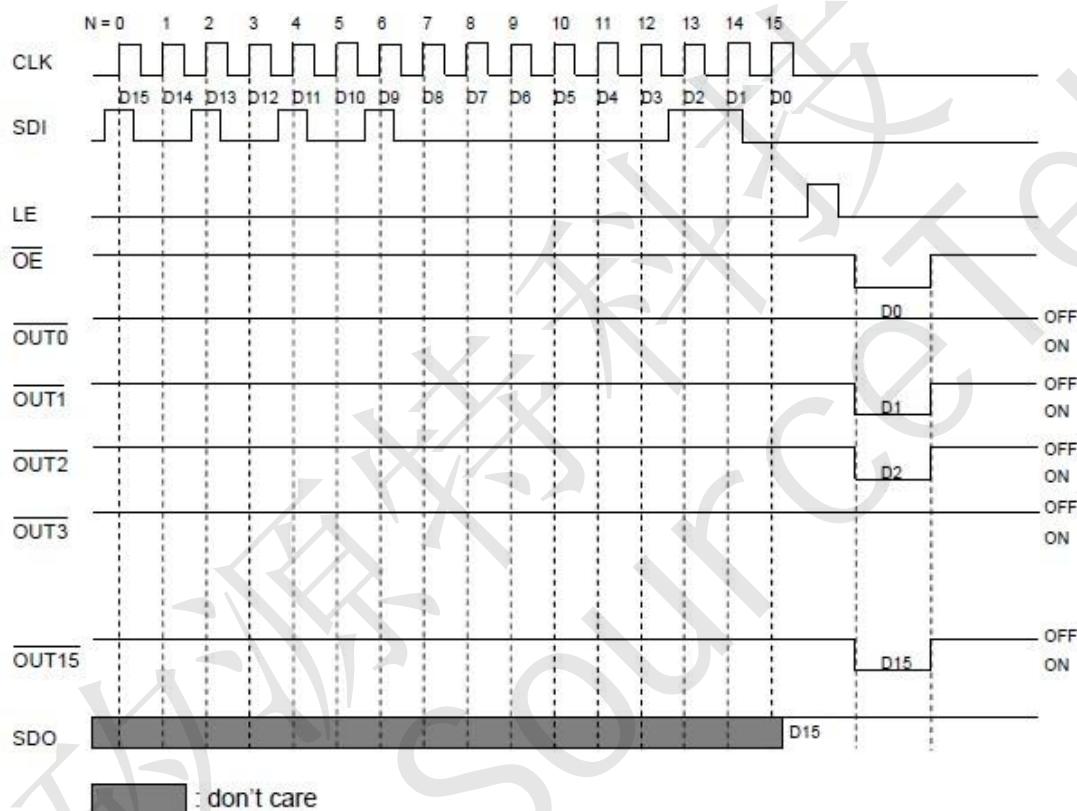
VI. CST5020D Truth Table

CLK	LE	OE/	SDI	OUT0~OUT15					SDO
↑	H	L	Dn	Dn	Dn-1	----	Dn-14	Dn-15	Dn-15
↑	L	L	Dn+1	unchanged					Dn-14
↑	H	L	Dn+2	Dn+2	Dn+1	----	Dn-12	Dn-13	Dn-13
↓	X	L	Dn+3	Dn+2	Dn+1	----	Dn-12	Dn-13	Dn-13
↓	X	H	Dn+3	Make LED not light up					Dn-13

VII. CST5020D Timing Diagram

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VIII. CST5020D Maximum Restricted Scope

characteristic		`symbol	Value	Unit
Power supply voltage		V_{DD}	0~7.0	V
input voltage		V_{IN}	-0.2~VDD+0.2	V
output current		I_{OUT}	36	mA/Channel
output withstand voltage		V_{OUT}	-0.2~11.0	V
Sum of earth terminal current		I_{GND}	510	mA
power dissipation	SOP24	P_D	1.92	W
	SSOP24		1.42	
	SSOP24-1.0		1.74	
	SDIP24		1.95	
thermal resistance value	SOP24	$R_{TH(j-a)}$	65	℃/W
	SSOP24		88	
	SSOP24-1.0		75	
	SDIP24		64	
Ambient temperature when the chip is working		T_{OPR}	-40~+85	℃
Ambient temperature during chip storage		T_{STG}	-55~+150	℃

● DC characteristic (V $_{DD}$ =5.0V)

Parameter		representative symbol	measurement condition		minimum value	typical value	Max	Unit
Power supply voltage		V_{DD}			4.5	5.0	5.5	V
output withstand voltage		V_{DS}	OUT0~OUT15		--	--	11.0	V
output current		I_{OUT}	Test circuit of reference DC characteristic		3	--	36	mA
		I_{OH}	SDO		--	--	-1.0	mA
		I_{OL}	SDO		--	--	1.0	mA
input voltage	high potential level	V_{IH}	Ta=-40~85℃		0.7"V_{DD}	--	V_{DD}	V
	low potential level	V_{IL}	Ta=-40~85℃		GND	--	0.3"V_{DD}	V
output leakage current		I_{OH}	V_{DS}=11.0V		--	--	0.5	uA
output voltage	SDO	V_{OL}	I_{OL} =+1.0mA		--	--	0.4	V
		V_{OH}	I_{OH} =-1.0mA		4.6	--	--	V
Output current 1		IOUT1	VDS=1.	Rext=6000Ω	--	3.13	--	mA

		0V				
current offset	dIOUT1	IOL=3.13mA VDS=1.0V	Rext=6000Ω	--	±1.5	±2.5	%
Output current 2	IOUT2	VDS=1.0V	Rext=735Ω	--	25.2	--	mA
current offset	dIOUT2	IOL=25.2mA VDS=1.0V	Rext=735Ω	--	±1.5	±2.5	%
Current Offset vs. Output Voltage	%/dVDS	Output voltage =1.0~3.0V		--	±0.1	--	%/V
Current Offset vs. Supply Voltage	%/dVDD	Power supply voltage =4.5~5.5V		--		±1.0	%/V
Pull-up resistance	RIN(up)	OE/		140	270	430	KΩ
Pull-down resistor	RIN(down)	LE		85	170	270	KΩ
Voltage source output current	OFF	$I_{DD}(off)1$	R ext = Not connected,OUT0 ~OUT15 =Off	--	2.3		mA
		$I_{DD}(off)2$	Rext=1250Ω,OUT0 ~OUT15 =Off		4.2		
		$I_{DD}(off)3$	Rext=625Ω,OUT0 ~OUT15 =Off	--	7		
	ON	$I_{DD}(on)1$	Rext=1250Ω,OUT0 ~OUT15 =On	--	4.5		
		$I_{DD}(on)2$	Rext=625Ω,OUT0 ~OUT15 =On	--	7		

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● **DC characteristic (V$_{DD}$ =3.3V)**

Parameter		representative symbol	measurement condition		minimum value	typical value	Max	Unit
Power supply voltage		V$_{DD}$			3.0	3.3	4.5	V
output withstand voltage		V$_{DS}$	OUT0~OUT15		--	--	11.0	V
output current		I$_{OUT}$	Ta=-40~85℃		3	--	20	mA
		I$_{OH}$	Ta=-40~85℃		--	--	-1.0	mA
		I$_{OL}$	SDO		--	--	1.0	mA
input voltage	high potential level	V$_{IH}$			0.7"V$_{DD}$	--	V$_{DD}$	V
	low potential level	V$_{IL}$			GND	--	0.3"V$_{DD}$	V
output leakage current		I$_{OH}$	V$_{DS=}$11.0V		--	--	0.5	uA
output voltage	SDO	V$_{OL}$	I$_{OL}$ =+1.0mA		--	--	0.4	V
		V$_{OH}$	I$_{OH}$ =-1.0mA		2.9	--	--	V
Output current 1		I$_{OUT1}$	V$_{DS}$=1.0V	R$_{ext}$=6000Ω	--	3.13	--	mA
current offset		dI$_{OUT1}$	I$_{OL}$=3.13mA V$_{DS}$=1.0V	R$_{ext}$=6000Ω	--	±1.5	±2.5	%
Output current 2		I$_{OUT2}$	V$_{DS}$=1.0V	R$_{ext}$=735Ω	--	25.2	--	mA
current offset		dI$_{OUT2}$	I$_{OL}$=25.2mA V$_{DS}$=1.0V	R$_{ext}$=735Ω	--	±1.5	±2.5	%
Current Offset vs. Output Voltage		%/dV$_{DS}$	Output voltage =1.0~3.0V		--	±0.1	--	%/V
Current Offset vs. Supply Voltage		%/dV$_{DD}$	Power supply voltage =3.0~3.6V		--		±1.0	%/V
Pull-up resistance		R$_{IN}$(up)	OE/		140	270	430	KΩ
Pull-down resistor		R$_{IN}$(down)	LE		85	170	270	KΩ
Voltage source output current	OFF	I$_{DD}$(off)1	R$_{ext}$ = Not connected,OUT0 ~OUT15		--	1.7		mA
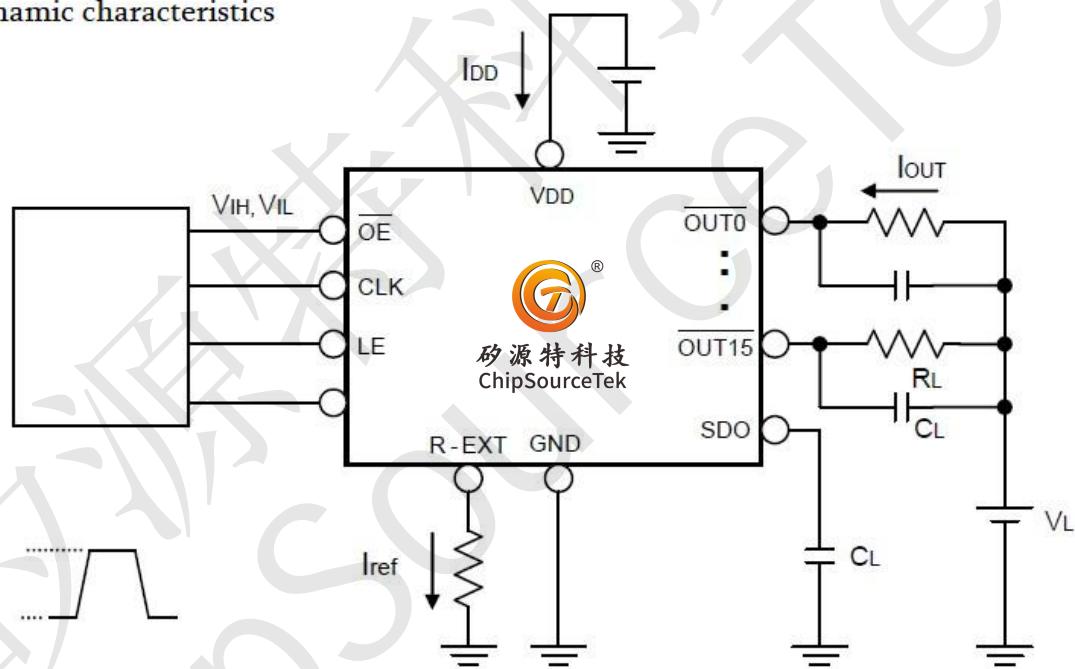
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		=Off			
	I_{DD}(off)2	R_{ext}=1250Ω,OUT0 ~OUT15 =Off		3.9	
	I_{DD}(off)3	R_{ext}=625Ω,OUT0 ~OUT15 =Off	--	6.2	
ON	I_{DD}(on)1	R_{ext}=1250Ω,OUT0 ~OUT15 =On	--	4.5	
	I_{DD}(on)2	R_{ext}=625Ω,OUT0 ~OUT15 =On	--	6.2	

Test circuit for dynamic characteristics

- **Dynamic characteristics (V $_{DD}$ =5.0V)**

characteristic		symbol	Test Conditions	minimum value	typical value	Max	Unit
CLK-OUT		tPLH1		--	35	55	ns
		tPHL1		--	35	55	ns
CLK-SDO		tPLH2	VDD=5.0V		32	51	ns
		tPHL2	VDS=1.0V		30	48	ns
OE-OUT		tPLH3	VIH=VDD		32	51	ns
		tPHL3	VIL=GND		32	51	ns
pulse width	CLK	tW(CLK)	Rext=930Ω	20	--	--	ns
	LE	tW(L)	VL=4.5V	20	--	--	ns

OE/	tW(OE)	RL=162Ω CL=10pF	50	100	--	ns
The Hold Time	tH(L)		30	--	--	ns
Setup Time of LE	tSu(L)		5	--	--	ns
SDI's Hold Time	th(D)		5	--	--	ns
SDI Setup Time	tsu(D)		3	--	--	ns
Maximum Climb Time of CLK Signal	tr		--	--	500	ns
Maximum falling time of CLK signal	tf		--	--	500	ns
Climb time for SDO	tr,SDO		--	10	--	ns
SDI Fall Time	Tf,SDO		--	10	--	ns
Potential ramp time of current output port	tor		--	35	--	ns
Potential fall time of current output port	tof		--	35	--	ns
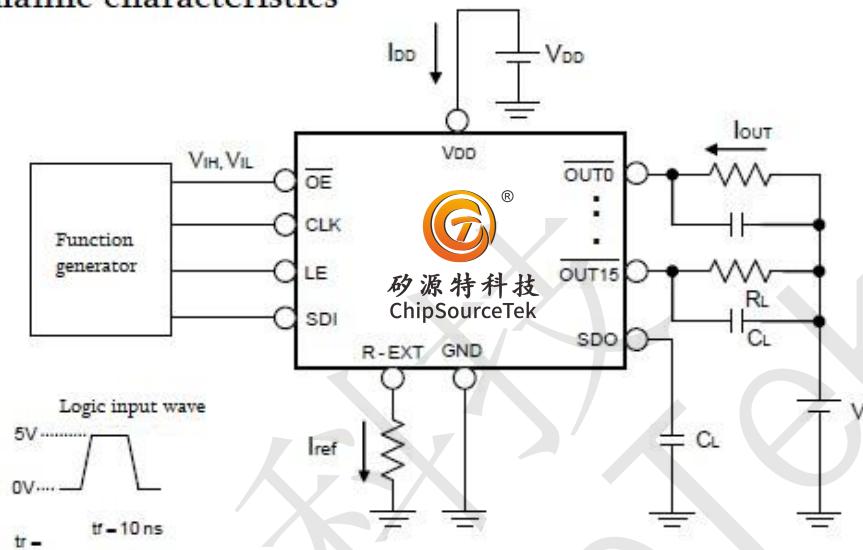
* This value is based on the shortest OE for which the output channels maintain a consistent response.

● Dynamic characteristics (V $_{DD}$ =3.3V)

characteristic		symbol	Test Conditions	minimum value	typical value	Max	Unit
CLK-OUT		tPLH1		--	35	55	ns
		tPHL1		--	35	55	ns
CLK-SDO		tPLH2			32	51	ns
		tPHL2			30	48	ns
OE-OUT		tPLH3			32	51	ns
		tPHL3			32	51	ns
pulse width	CLK	tW(CLK)	VDD=5.0V VDS=1.0V VIH=VDD VIL=GND Rext=930Ω VL=4.5V RL=162Ω CL=10pF	20	--	--	ns
	LE	tW(L)		20	--	--	ns
	OE/	tW(OE)		50	100	--	ns
The Hold Time		tH(L)		30	--	--	ns
Setup Time of LE		tSu(L)		5	--	--	ns
SDI's Hold Time		th(D)		5	--	--	ns
SDI Setup Time		tsu(D)		3	--	--	ns
Maximum Climb Time of CLK Signal		tr		--	--	500	ns
Maximum falling time of CLK signal		tf		--	--	500	ns
Climb time for SDO		tr,SDO		--	10	--	ns
SDI Fall Time		Tf,SDO		--	10	--	ns
Potential ramp time of current output port		tor		--	35	--	ns
Potential fall time of current output port		tof		--	35	--	ns

Test circuits for dynamic characteristics
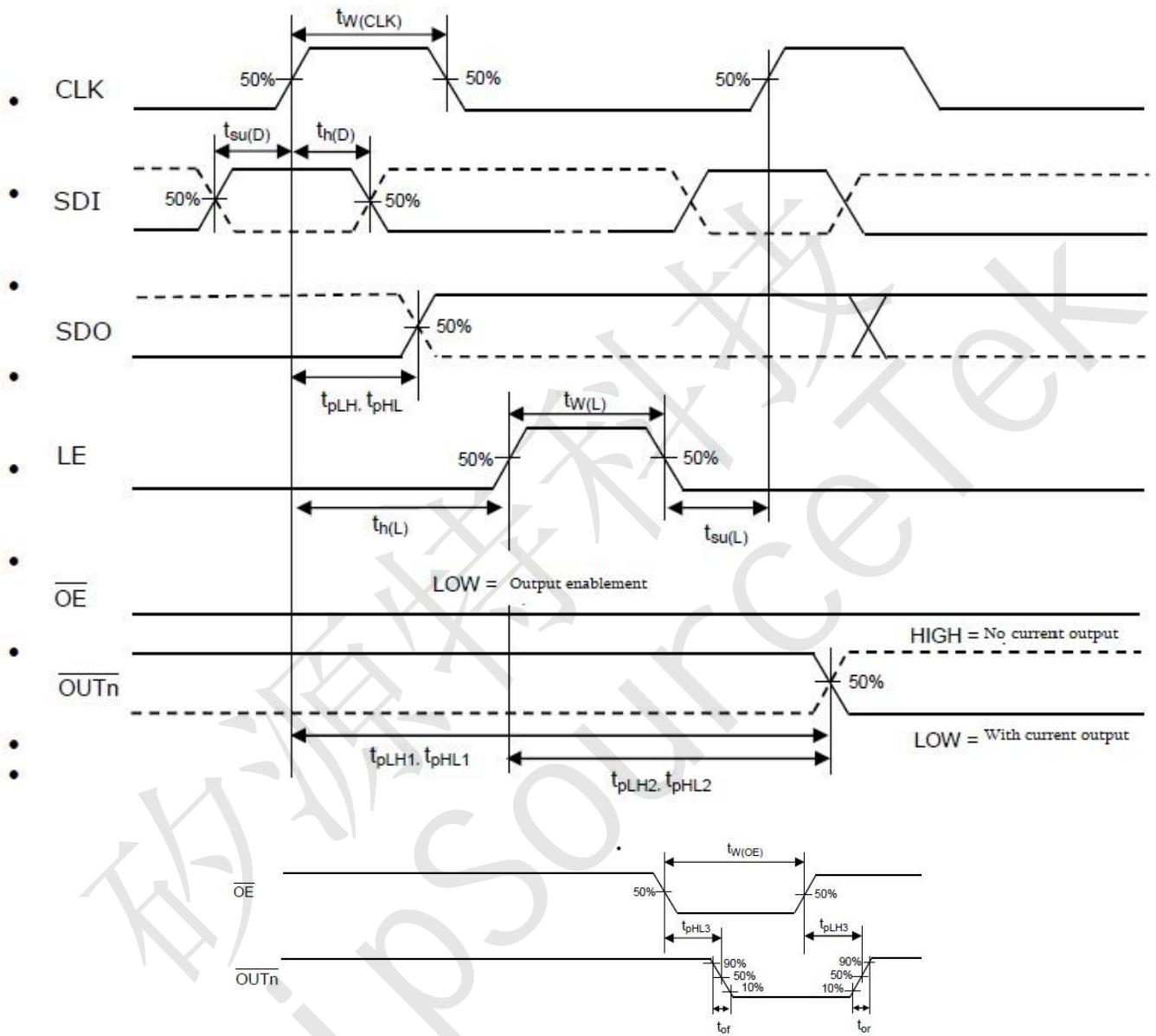
IX. CST5020D Waveform Diagram of Time Sequence

X. CST5020D Application Information

■ **constant current**
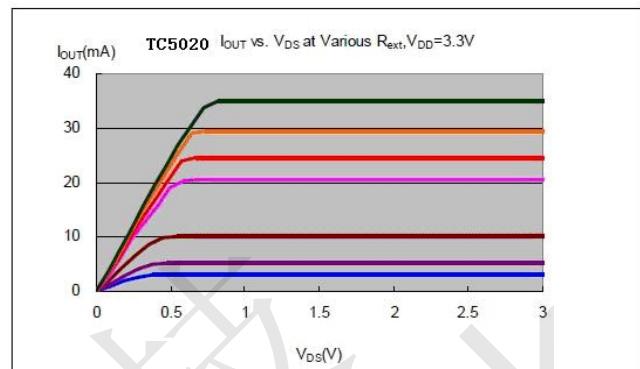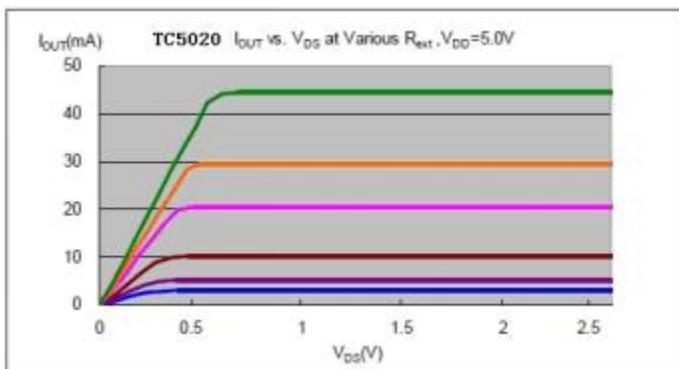
When customers apply the CST5020D to LED display designs, the current between channels and even between chips is very small. This is due to the excellent properties of CST5020D:

➤ The maximum current difference between channels is less than ±2.5%, and the maximum current difference between chips is less than ±3%.

➤ The current output characteristic is independent of the voltage at the load terminal, as shown in the figure below. Output current stability will not be affected by LED forward voltage (VF) changes

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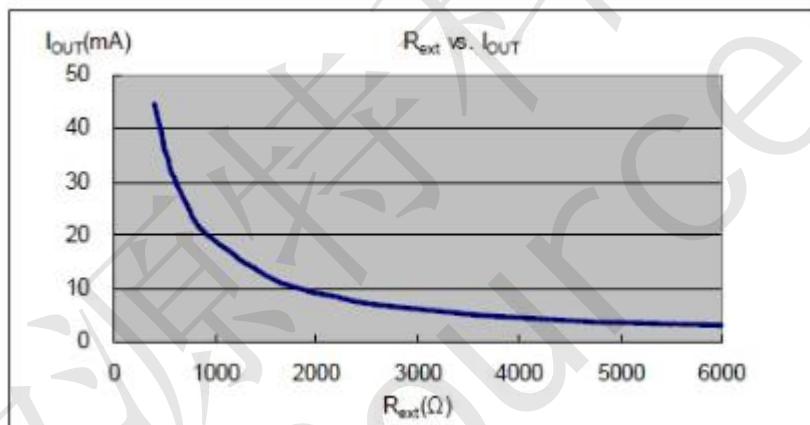
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■ Adjust the output current

The output current (IOUT) is adjusted by an external resistor, Rext, as shown in the figure below.

The output current value can be calculated by applying the following formula.

$VR\text{-}EXT = 1.21V; IOUT = VR\text{-}EXT*(1/Rext) \times 15; Rext = (VR\text{-}EXT/IOUT) \times 15$

VR-EXT is the voltage at R-EXT and Rext is the resistor externally connected to R-EXT. When the resistance value is 744Ω, the output current value of 24.4mA can be obtained through the calculation of the formula; When the resistance value is 1860Ω, the output current is 9.8mA.

■ "Pb-Free & Green"
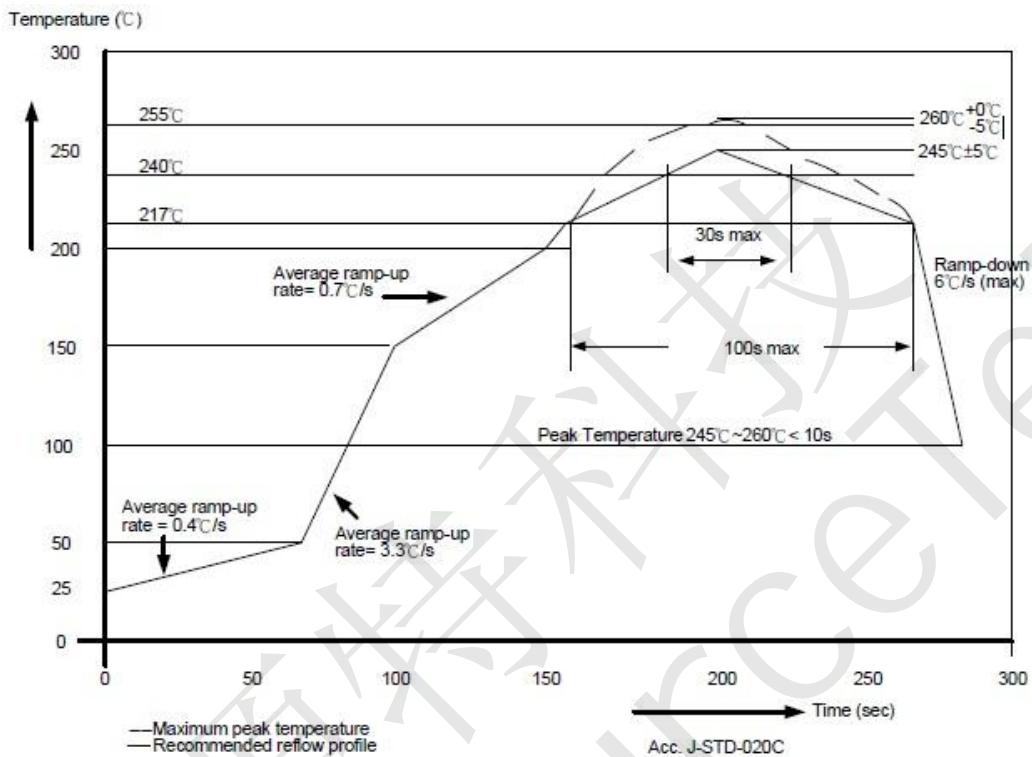
The Pb-Free Green semiconductor products manufactured by Fumon Electronics& comply with the European RoHS standard, and the package is 100% pure tin to be compatible with the current tin-lead (SnPb) soldering process, and support the lead-free process that requires higher temperature. Pure tin has been widely used by electronic products customers and suppliers in Europe, America and Asia, and has become the best substitute for tin-containing lead materials. 100% pure tin can be produced in tin-lead (SnPb) furnace processes at process temperatures of 215 ° C to 240 ° C. However, if the customer uses completely lead-free solder paste

and materials, the solder furnace temperature must be 245 ° C to 260 ° C according to J-STD-020C standard (refer to the figure and table below).

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≥2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≥2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

Note: For details, please refer to the "Policy on Pb-free Green Package" of Accumulate Technology&.
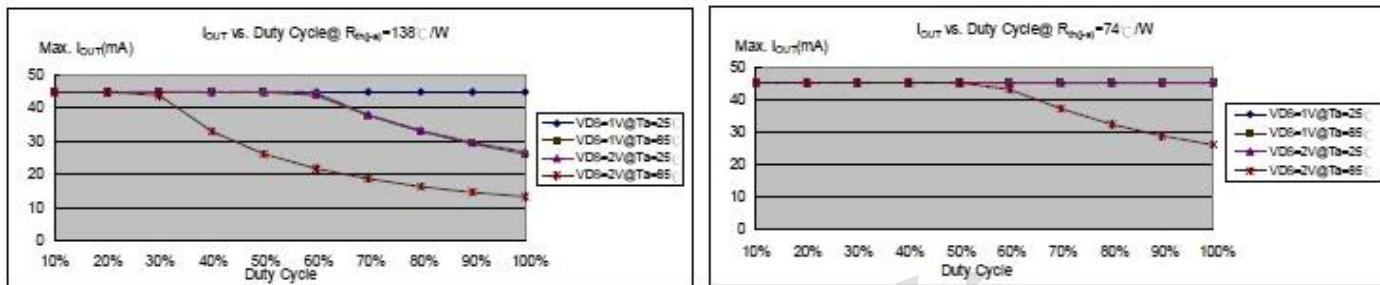
■ Package Thermal Power (P $_D$)

The maximum heat dissipation power of the package is determined by the formula PD(max)=(Tj-Ta)/Rth(j-a). When 16 channels are on at the same time, the true power is PD(act)=(IDDxVDD)+(IOUTxDutyxVDSx16). To keep PD(act)≤PD(max), the relationship between the maximum current that can be output and the duty cycle is: IOUT={[(Tj-Ta)/Rth(j-a)]-(IDDxVDD)}/VDS /Duty/16, where Tj=150°C.
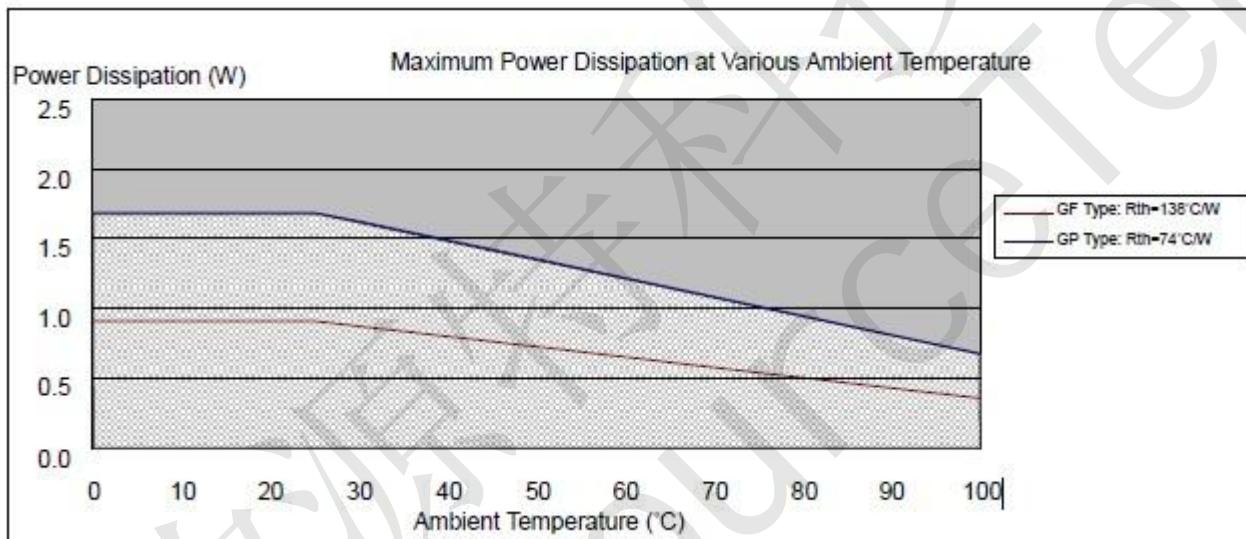
According to PD(max)=(Tj-Ta)/Rth(j-a), the maximum allowable heat dissipation power decreases as the ambient temperature increases.

Maximum Power Dissipation at Various Ambient Temperature

■ **Supply voltage at load side (V $_{LED}$)**

To optimize package heat dissipation, the recommended operating range for the output voltage (V $_{DS}$) is 0.4V to 0.8V(I $_{OUT}$ =3 to 45mA). What if

When V $_{DS}$ =V $_{LED}$-V $_F$ and V $_{LED}$ =5V, an excessively high output voltage (V $_{DS}$) may cause P$_D$ (act)>P $_D$ (max); in this case, it is recommended to use
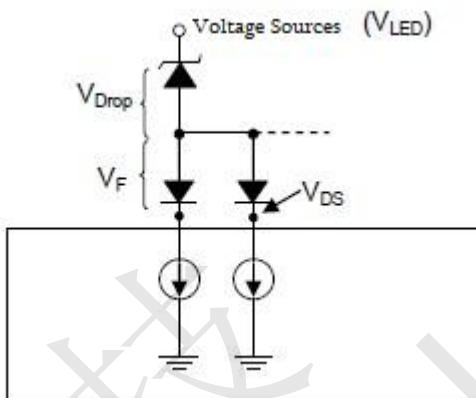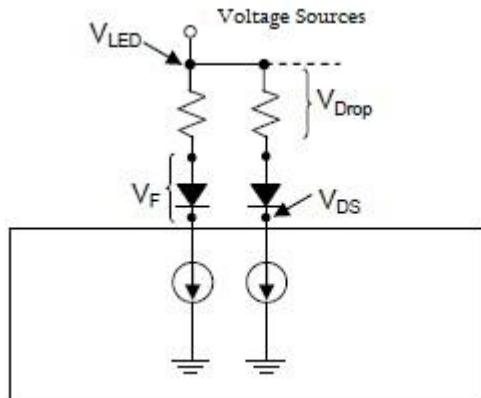
For lower V $_{LED}$ voltage supplies, an external string resistor or Zener diode can also be used as V $_{DROP}$. This results in V $_{DS}$ =(V $_{LED}$-V $_F$)-V $_{DROP}$, which reduces the output

Effect of terminal voltage (V $_{DS}$). An application diagram of an external series resistor or Zener can be found in the following figure.
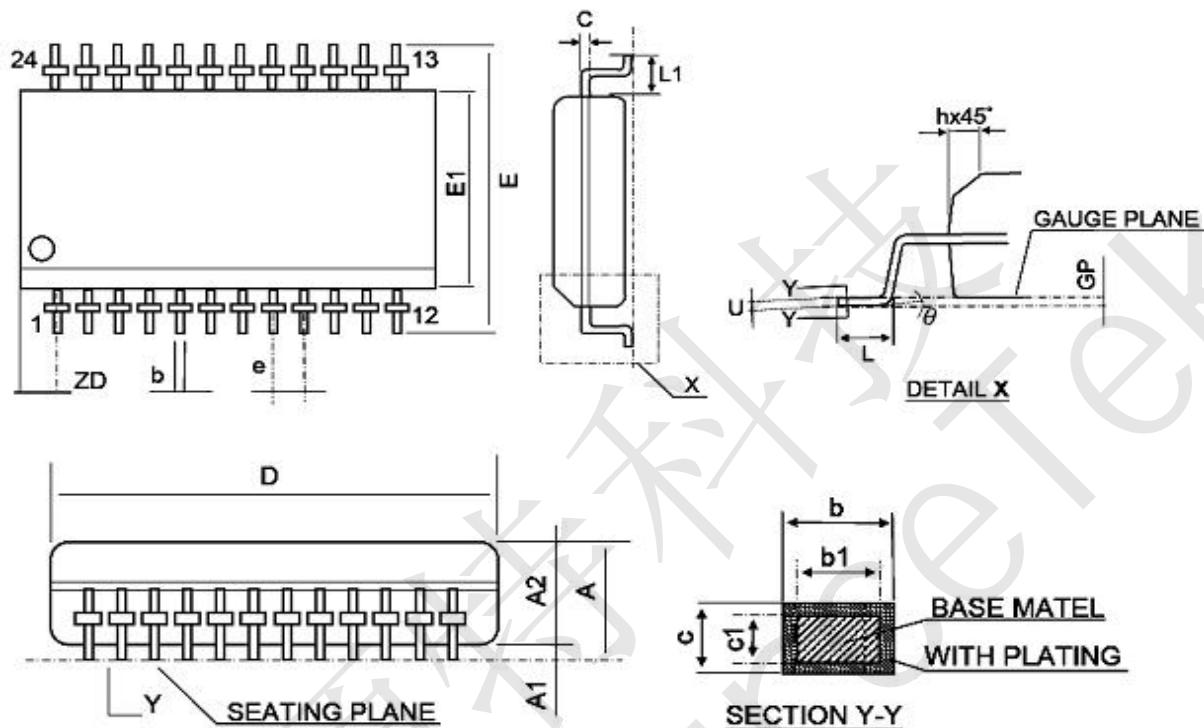
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XI. CST5020D Package size drawing

SSOP24-0.635
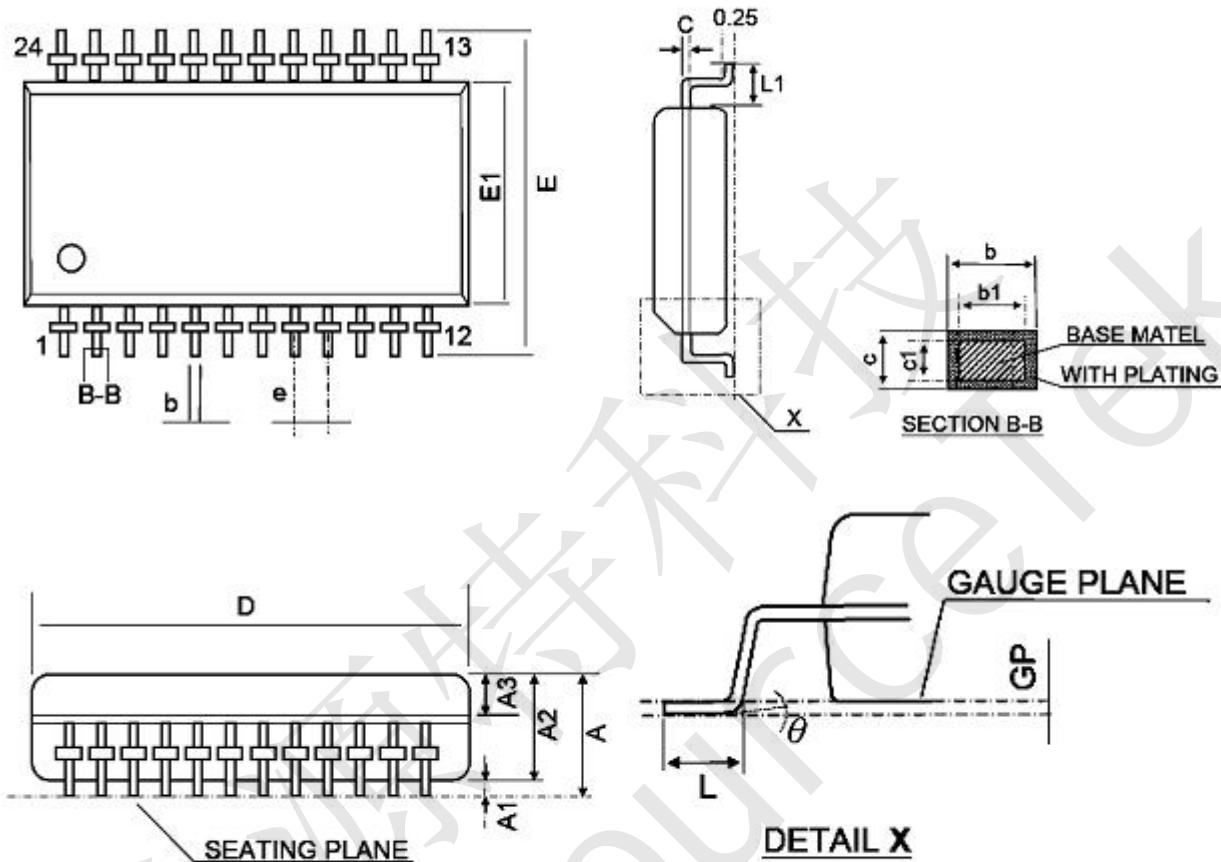
SYMBOL	DIMENSION (mm)			DIMENSION (mil)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2			1.50			59
b	0.20		0.30	8		12
b1	0.20	0.254	0.28	8	10	11
c	0.18		0.25	7		10
c1	0.18	0.203	0.23	7	8	9
D	8.56	8.66	8.74	337	341	344
E	5.80	6.00	6.20	228	236	244
E1	3.80	3.90	4.00	150	154	157
e	0.635 BSC			25 BSC		
h	0.25	0.42	0.50	10	17	20
L	0.40	0.635	1.27	16	25	50
L1	1.00	1.05	1.10	39	41	43
ZD	0.838 REF			33 REF		
Y			0.10			4
θ	0°		8°	0°		8°

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SSOP24-1.0

SYMBOL	DIMENSION (mm)			DIMENSION (mil)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	2.20	-	-	87
A1	0.10	0.20	0.30	4	8	12
A2	1.60	1.80	2.00	63	71	79
A3	0.62	0.82	0.92	24	32	36
b	0.39	-	0.47	15	-	19
b1	0.38	0.40	0.43	15	16	17
c	0.15	-	0.20	6	-	8
c1	0.14	0.15	0.16	5.5	6	6.5
D	12.80	13.00	13.20	504	512	520
E	7.70	7.90	8.10	303	311	319
E1	5.80	6.00	6.20	228	236	244
e	1.00 BSC			39 BSC		
L	0.35	0.45	0.55	14	18	22
L1	0.95 BSC			37 BSC		
θ	0°	-	8°	0°	-	8°