



CST20P02

P-Ch 20V Fast Switching MOSFETs

- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

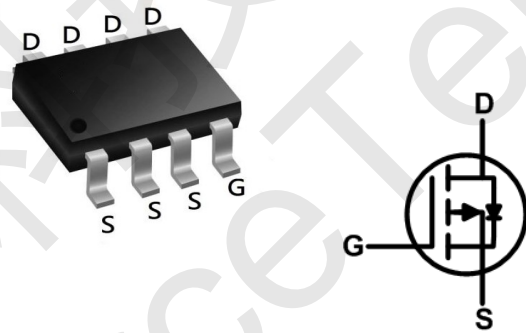


BVDSS	R <sub>DS(on)</sub>	ID
-20V	15 mΩ	-20A

Description

The CST20P02 is the high cell density trenched P-ch MOSFETs, which provide excellent R<sub>DS(on)</sub> and gate charge for most of the synchronous buck converter applications. The CST20P02 meet the RoHS and Green Product requirement with full function reliability approved.

SOP8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	-20	V
V <sub>GS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup>	-20	A
I <sub>D</sub> @T <sub>C</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup>	-18	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	-68	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>3</sup>	18	W
P <sub>D</sub> @T <sub>C</sub> =70°C	Total Power Dissipation <sup>3</sup>	12	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	75	°C/W
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup> (t ≤ 10s)	40	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	4.2	°C/W



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Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.012	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-4.5V, I_D=-10A$	---	15	19	$m\Omega$
		$V_{GS}=-2.5V, I_D=-8A$	---	19	23	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.4	-0.7	-1.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.94	---	$mV/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-15V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-10A$	---	43	---	S
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-10V, V_{GS}=-4.5V, I_D=-10A$	---	35	---	nC
$Q_{gs}$	Gate-Source Charge		---	5.0	---	
$Q_{gd}$	Gate-Drain Charge		---	10	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-10V, V_{GS}=-4.5V,$ $R_G=3.3\Omega, I_D=-10A$	---	12.0	---	ns
$T_r$	Rise Time		---	40.0	---	
$T_{d(off)}$	Turn-Off Delay Time		---	30	---	
$T_f$	Fall Time		---	10	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	2800	---	pF
$C_{oss}$	Output Capacitance		---	690	---	
$C_{riss}$	Reverse Transfer Capacitance		---	590	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	-20.0	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	---	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=-10A, dI/dt=100A/\mu s,$	---	27	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	17.8	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 4.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.



CST20P02

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Typical Characteristics

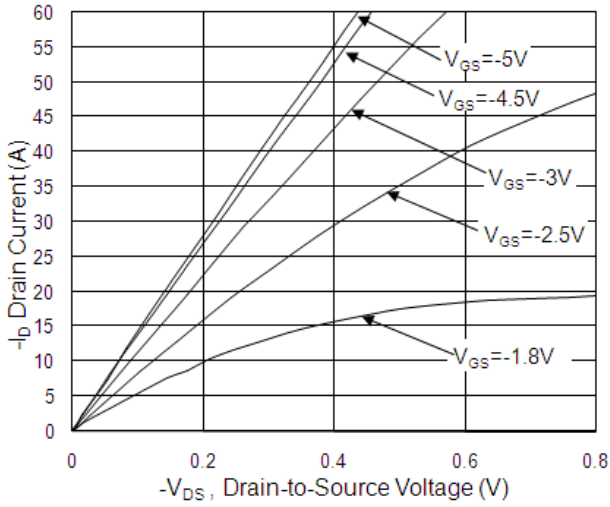


Fig.1 Typical Output Characteristics

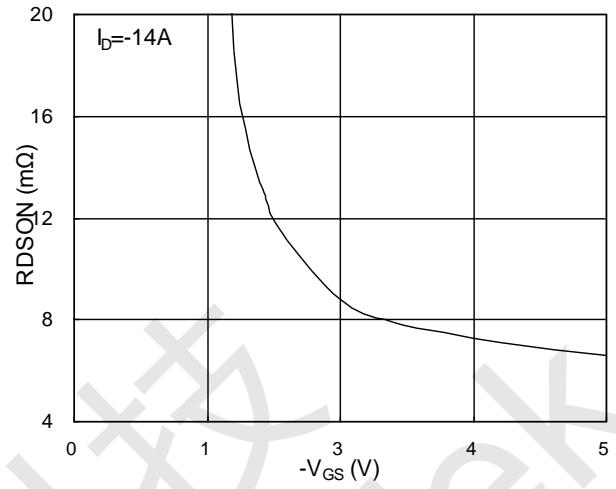


Fig.2 On-Resistance vs. G-S Voltage

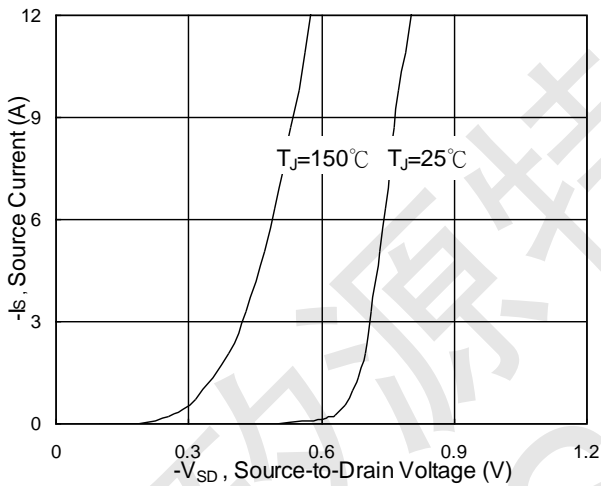


Fig.3 Forward Characteristics of Reverse

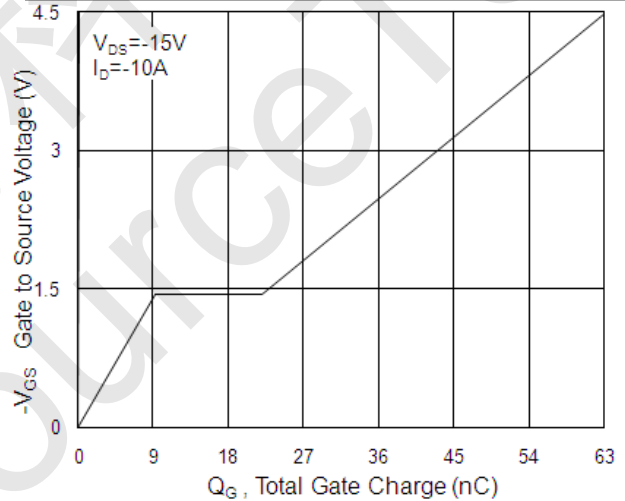


Fig.4 Gate-charge Characteristics

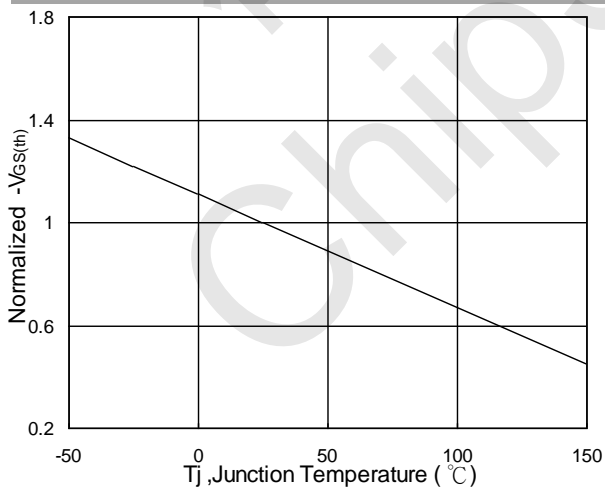


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

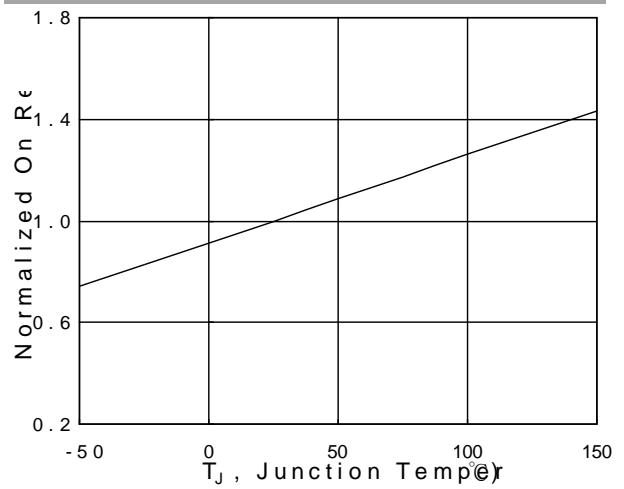


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



CST20P02

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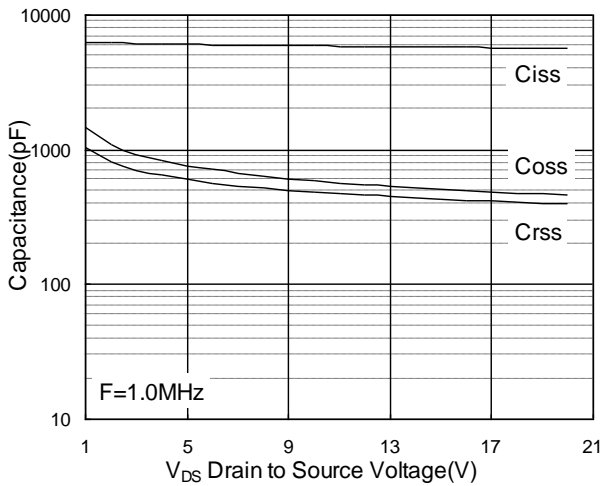


Fig.7 Capacitance

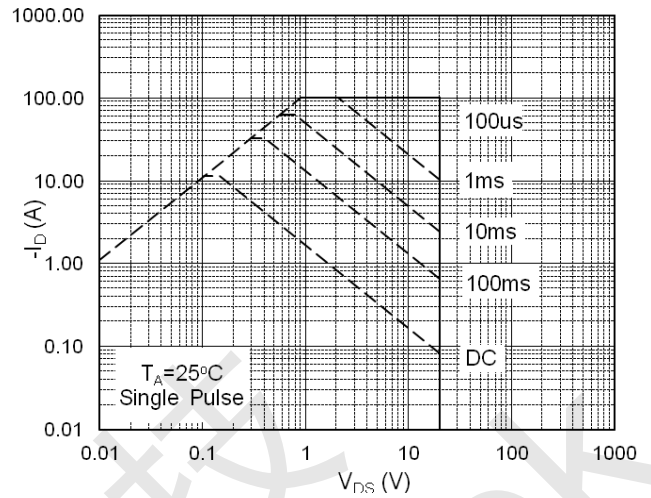


Fig.8 Safe Operating Area

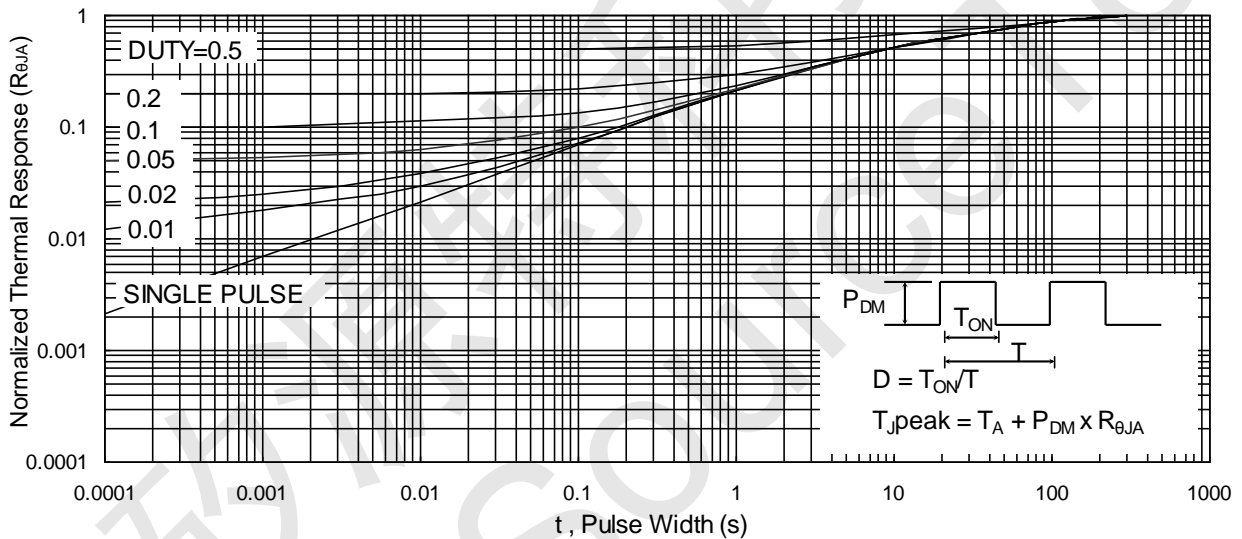


Fig.9 Normalized Maximum Transient Thermal Impedance

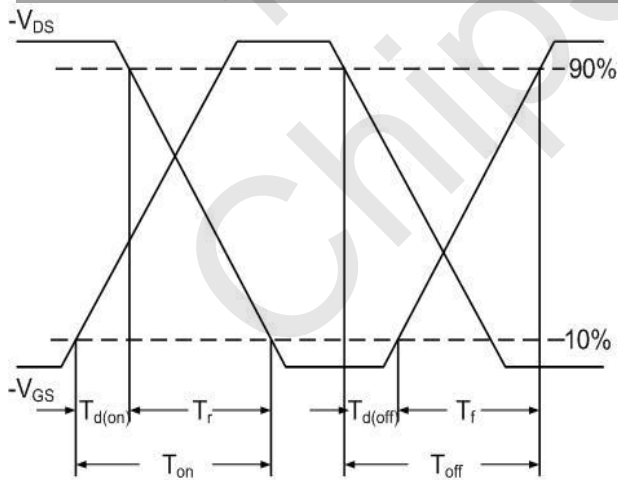


Fig.10 Switching Time Waveform

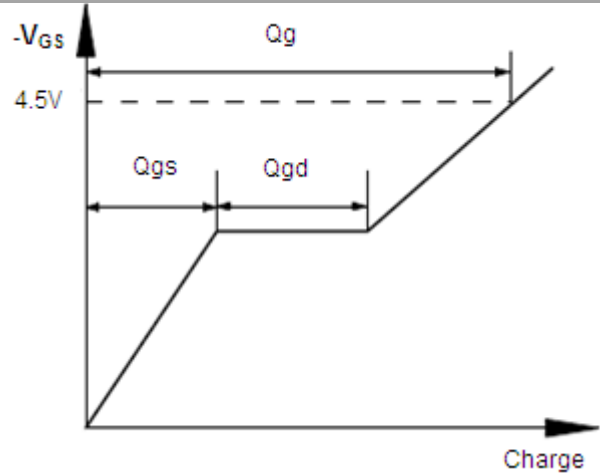


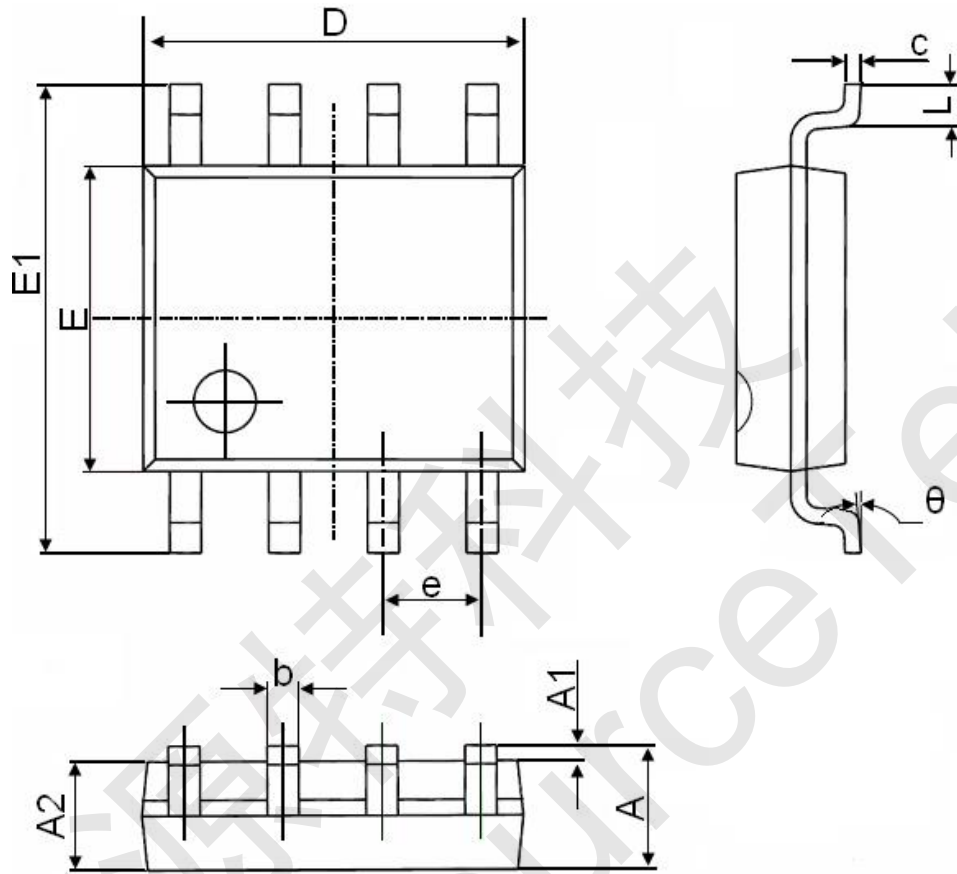
Fig.11 Gate Charge Waveform



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SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°