CST16P161A

Data Sheet

V1.3

12K Embedded OTP ROM

Hi-Performance 16-bit Multimedia Processor

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1. CST16P161A General Description

The **TxP16**™ is a high performance 16-bit MCU, pronounced as **T**ritan e**x**cellent-**P**rocessor16. It is the new generation computational kernel for CST16P161A series. It has initially aimed at the areas of controller and multimedia digital signal processing (DSP) application to demonstrate its profession. TxP16 furnish with fast **MAC** architecture, which allows multiplication+accumulation instructions to be issued with access memory simultaneously during one cycles. The CST16P161A is equipped with TxP16 and integrating input/output ports, PWM, Timer and Low Voltage Reset...etc on a chip.

Furthermore, CST16P161A extend its external device connection capability such as Serial ROM/Flash and UART. The internal memory capacity includes 12Kx16 program/data OTP ROM plus 3072x16 working SRAM.

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2. CST16P161A Features

- High-performance RISC TxP16 CPU
  - **13Mhz@2.4Volt ~ 5.5Volt , 11Mhz@2.4Volt ~ 5.5Volt or 6.5Mhz@2.4Volt ~ 5.5Volt**
  - Built-in 3072x16 SRAM
  - Hybrid Instruction and data memory share with 12Kx16 OTP ROM
  - Embedded PC Stack Level 16
- Rich DSP function
  - Hardware Circular Buffer support
  - MAC Computation power : 13MIPS (max.)
  - Multi-Function Support: In MAC calculation, simultaneously access two operands from memory in one cycle
  - Extend Dynamic Range: A 40-bit accumulator to ensure in 512 successive multiple+additions no overflows
- Software-based audio processing technical
  - ADPCM , CELP , Melody synthesis up to 12channels (Max)
- System Clock : RC oscillator **65.536MHz±1%**
- **Support 24 general purpose I/O port**
- Stereo 16-bit PWM
- Advanced Interrupt System
  - 6 internal interrupt (PWM, T1, T2, RTC, SPI, StackOvl)
  - 3 external interrupt
  - FIRQ
- Built-in UART/IR
- SPI Master Interface
- Timer1 , Timer2 with External I/O Pin Trigger
- Support Spread Spectrum clocking to reduce EMI
- Mono DAC
- ADC 10bit / 71.2 kbps(@ACQT = 4*TAD and FADC=1Mhz) / 8 channel
- Microphone pre-amplifier circuit
- Low battery detector(The accuracy of low battery detector is ± 4%)
- Anti-noise Touch Key detecting circuit
- Support External 32768 Crystal
- Watch dog timer (WDT)
- Low voltage reset (LVR)
- **Low dropout regulator(LDO V28O) supply 2.9V@20mA (voltage drop 0.1v)**
- **PB0,PB1 support two edge modes for wake-up function are rising and falling edge trigger. The rising and falling edge trigger is selected by option.**
- **Port C support 4 comparators**
- **built-in low power RC oscillator 32768Hz±2%, for 0.0625ms, 0.125ms, 0.25ms, 1ms, 2ms, 4ms, 8ms and 128ms, wakeup or real time clock use. RC oscillator can be disable by option.**
- **Compatible PWM driver: CST1309CP**

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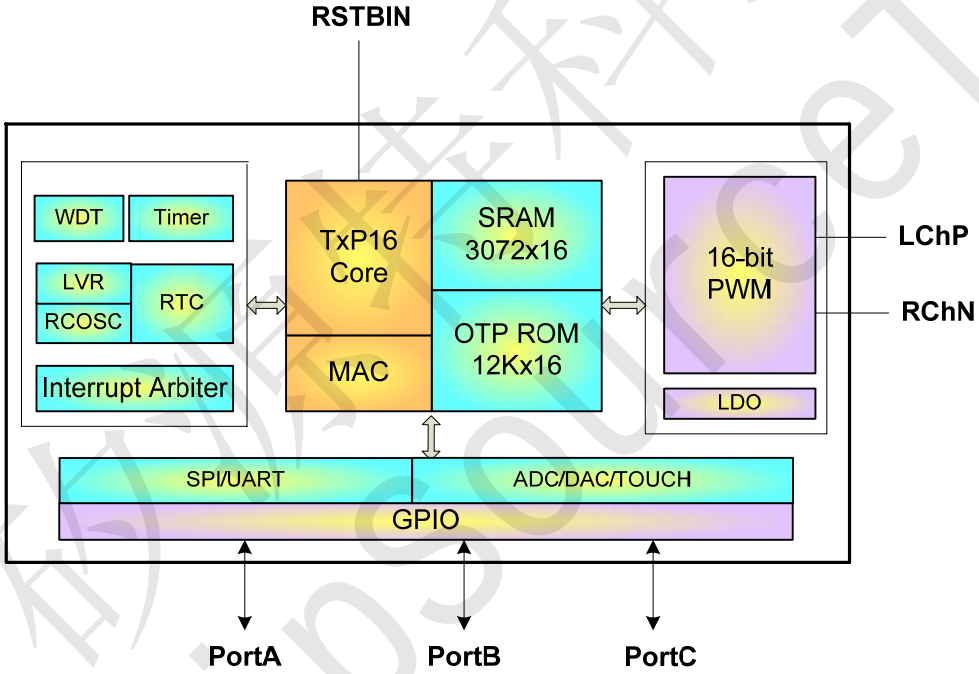
3. CST16P161A Application Field

- PDA
- Electronic Dictionary
- Handheld Games
- Electronic Learning Aid (ELA)
- Digital Photo Frame
- Electronics storybook

4. CST16P161A Block Diagram



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4.1. Pin Assignments /Description

Pin Name	I/O	State after RESET	FUNCTIONS
Chip Power			
VCC	I	High	Chip Power Input
GND	I	Low	Digital Ground
AVSS	I	Low	Analog Ground
VIO	I	High	PortA IO PAD Power Input
VSS	I	Low	IO Block Ground
VPPX	I	U	OTP programming Power Supply 7.5V
VPD	I	High	PWM PAD Power Input
VPS	I	Low	PWM PAD Ground
VIO2	I	High	PortB IO PAD Power Input
V28O	O	High	**LDO 2.9V Power Output For SPI Flash**
Chip Control			
TESTIN	I	Low	High force chip enter test mode, internal 50K ohm pull-down
HALT	O	Low	High presents chip in Halt mode
RSTBIN	I	High	Low force chip to enter reset mode, internal 50K ohm pull-up
General Purpose I/O Port			
PortA[7:0]	I/O	Low	PortA is programmable Input/Output port
PortB[7:0]	I/O	Low	PortB is programmable Input/Output port
PortC[7:0]	I/O	Low	PortC is programmable Input/Output port
PWM Audio			
PWMP	O	Low	Digital PWM output(+)
PWMN	O	Low	Digital PWM output(-)

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5. CST16P161A Function Descriptions

5.1 TxP16

As shown in the block diagram in Figure 4.1, the TxP16 with MAC module is a 16-bit data width processing capability and all instructions are operated in one cycle except parameter data ROM(PM) access. The TxP16 not only provides general arithmetic such as addition, subtraction, shifter, and other logical operations, but it also involves MAC and circular buffer operations for complexity digital signal processing.

5.2 TxP16 Registers

The TxP16 contains of register files are illustrated below:

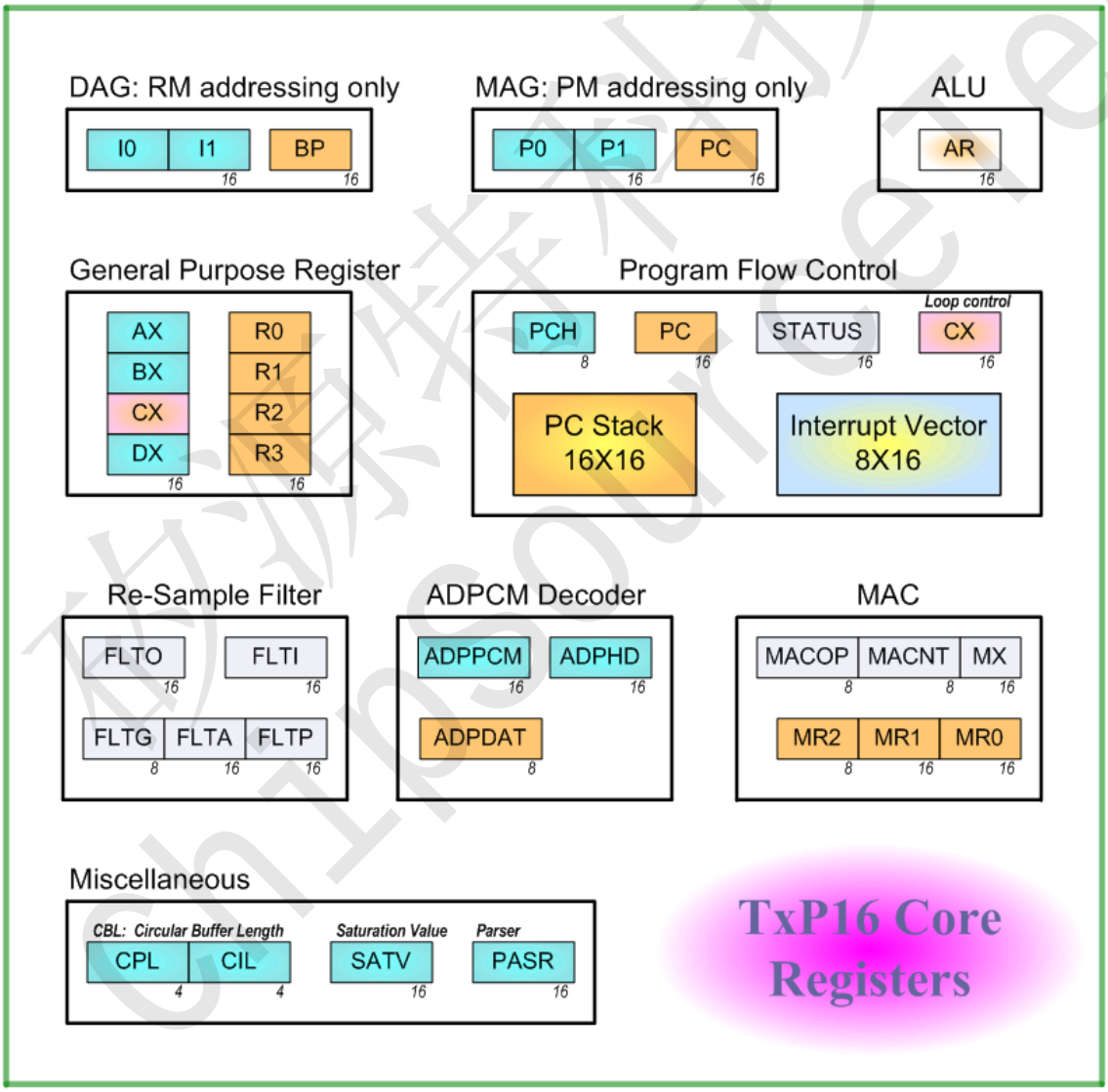

Figure 5.1 TxP16 Processor Core Registers

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■ REGISTER FILES DEFINE:

AR: Accumulator Register
I0: Index 0 Register
I1: Index 1 Register
BP: Base Pointer Register
P0: Pointer 0 Register
P1: Pointer 1 Register
MACOP: MAC Operation Register
MACNT: MAC Operation Loop Counter
MX: MUL/MAC Input X Register
MR0: MUL/MAC Result Register 0
MR1: MUL/MAC Result Register 1
MR2: MUL/MAC Result Register 2
AX: General AX Register
BX: General BX Register
CX: General CX Register
DX: General DX Register
R0: General R0 Register
R1: General R1 Register
R2: General R2 Register
R3: General R3 Register
CBL: Circular Buffer Length Register
PASR: Parser Register

5.2.1 Special Registers

- Accumulator Register

The AR is a general-purpose 16-bit register that stores the result of last arithmetic or logical operation. In addition, any data write to AR will affect the status flag.

- Stack Pointer

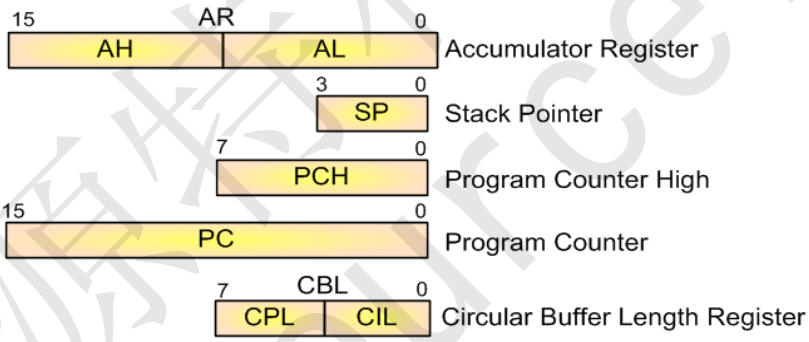

Figure 5.2 TxP16 Special Registers

The SP is a 4-bit register that is for addressing Stack position. The SP will automatically increment / decrement cause by instruction “CALL” / “RETS”, and more detail revealed as the “PC Stack” section.

- Program Counter

The 16-bit PC register provides 64K-word addressing capability. It is responsible for MCU fetch now executing instruction.

- Program Counter High

The instruction “LJMP” and “LCALL” will reference PCH register to composed of 16-bit pointer provides the 64K words PM addressing range.

- Circular Buffer Length Register

Many algorithms such as convolution, correlation, and digital filter require the circular data buffers. The TxP16 supports circular buffer operating via the I0 vs. CIL and P0 vs. CPL. The modulus logic implements automatic modulus addressing for accessing RM/PM circular buffer data.

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5.2.2 Common I/O Registers

The TxP16 involves 32 common I/O registers are shown in Table 5.1. There are defined the peripheral IO control and system register.

Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
STATUS.L	00H	20	R/W	INTEN			AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR				UART_EN	SPI_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Interrupt Enable
INTENA.H	01H	00	R/W	-	-	-	-	-	-	-	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
INTREQ.H	02H	00	R/W	-	-	-	-	-	-	-	Req8	
IntVect	03H	XX	R/W	IntVect[15:0]								Interrupt Vector access Window
IOC_PA	04H	00	R/W	IOC_PA[7:0]								"1"= out, "0" = in of related PA bit
IOC_PB	05H	00	R/W	IOC_PB[7:0]								"1"= out, "0" = in of related PB bit
IOC_PC	06H	00	R/W	IOC_PC[7:0]								"1"= out, "0" = in of related PC bit
PortA	07H	XX	R/W	PortA[7:0]								Read: in port Write: out port
PortB	08H	XX	R/W	PortB[7:0]								Read: in port Write: out port
PortC	09H	XX	R/W	PortC[7:0]								Read: in port Write: out port
	0AH	XX	R/W									Read: in port Write: out port
Reserve	0BH	XX	W									Read: In, Write: Out Data
Reserve	0CH	XX	XX									"1"= out, "0" = in of related PD bit
SPI_CTL	0DH	XX	R/W	SPI_CFG [15:0]								SPI Signal
SPI_DAT	0EH	XX	R/W	SPI_DAT [15:0]								SPI Signal
INTMASK.L	0FH	00	R/W	Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0	Interrupt Mask
INTMASK.H	0FH	00	R/W	-	-	-	-	-	-	-	Mask8	
Reserve	10H	XX	R/W									
Reserve	11H	XX	R/W									
UART_CTL	12H	XX	XX	UART_CTRL[15:0]								
UART_DAT	13H	XX	XX	UART_DATA[15:0]								
Reserve												
Reserve	15H	00	R/W									
DACL	16H	XX	R/W	DACL [15:0]								Audio L Channel
DACR	17H	XX	W	DACR [15:0]								Audio R Channel
DACTL	18H	00	R/W								PwmMT	"1"= Mute
Reserve	19H	XX	XX									Reserve
Reserve	1AH	XX	XX									Reserve
MISC2.L	1BH	00	R/W	*7	*6	*5	*4	*3	*2	*1	-	
MISC2.H	1BH	00	R/W	*15	*14	*13	*12	*11	*10	*9	*8	
MISC.L	1CH	0X	R/W			PWM_SR	PWM_4K	POWON (R)	EXRST (R)	LVR (R)	WDT (R)	System Reset source come from
MISC.H	1CH	00	R/W			*21	*20	*19	*18	*17	*16	
ClrWDT	1DH	XX	W									Clear WDT
RealT	1DH	00	R	RealT[15:0]								Watch Dog Real-Time Counter
IOP_IX	1EH	XX	W	IOPIX7	IOPIX6	IOPIX5	IOPIX4	IOPIX3	IOPIX2	IOPIX1	IOPIX0	Programming IO Port index/
IOP_DAT	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

*1: PWMPIO_EN *2 PWMNIO_EN *3 PWMIO_MODE *4: EXTINT0_PIN_SEL

*5 EXTINT0_PIN_INV *6: EXTINT1_PIN_SEL *7: EXTINT1_PIN_INV *8: EXTTIMER1_PIN_SEL

*9: EXTTIMER1_PIN_INV *10: EXTTIMER2_PIN_SEL *11: EXTTIMER2_PIN_INV *12: FIRQ_PIN_SEL

*13: FIRQ_PIN_INV *14: SPI_NEW_MODE *15: INT_MASK_EN *16: EXTINT0_DoubleT_En

*17: EXTINT1_DoubleT_En *18: EXTINT2_DoubleT_En *19: EXTINT2_INT_En *20: EXTINT2_PIN_SEL

*21: EXTINT2_PIN_INV

Table 5.1 Common I/O registers

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5.2.3 Basic System Registers

◆STATUS register

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS.L	00H	20	R/W	INTEN			AQ	AN	AV	AC	AZ	
STATUS.H	00H	00	R/W	PA	FA	IntVWR				UART_EN	SPI_EN	System Status Flag

The Status register provides two main functions, the first system flag holds the status information generated by the computational blocks of the TxP16, which used for program sequencer control. The second indicated that special function of hardware module is enable or not.

For program flow control:

System Flag	Definition
AZ	ALU or AR Result Zero
AN	ALU or AR Result Negative
AV	ALU Overflow
AC	ALU Carry
PA	Parser Queue available(Read only)
FA	Filter buffer available(Read only)

System hardware control:

System Flag	Definition
INTEN	System global interrupt control bit
IntVWR	Interrupt Vector Table access window control bit
UART_EN	UART interface enable control bit
SPI_EN	Serial peripheral interface enable control bit

◆ Address 01H~02H: Interrupt control registers, the detail are illustrated in Interrupt section.

◆ Address 04H~15H: GPIO registers, the detail are illustrated in GPIO section.

◆Address 16H~18H: DAC control registers, the detail are illustrated in AUDIO section.

◆System Miscellanea register

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC.L	1CH	0X	R/W			PWM_SR	PWM_4K	POWON (R)	EXRST (R)	LVR (R)	WDT (R)	System miscellanea register
MISC.H	1CH	00	R/W			*6	*5	*4	*3	*2	*1	

The system MISC[3:0] register indicates which one is the reset source before DSP system re-boot.

MISC register	Definition
EXTINT2_PIN_INV (*6)	External Interrupt 2 Input Pin Inverse
EXTINT2_PIN_SEL (*5)	External Interrupt 2 Pin Select: 0(PA3), 1(PC5)
EXTINT2_INT_En (*4)	External Interrupt 2 Enable bit
EXTINT2_DoubleT_En (*3)	External Interrupt 2 Double Edge Trigger Enable bit
EXTINT1_DoubleT_En (*2)	External Interrupt 1 Double Edge Trigger Enable bit
EXTINT0_DoubleT_En (*1)	External Interrupt 0 Double Edge Trigger Enable bit
PWM_4K	Audio PWM Interrupt Frequency 4K Enable bit
PWM_SR	Audio PWM Sampling-Rate: 0(32K), 1(64K)
POWON	System Reset from power on
EXRST	System Reset from external reset pin
LVR	System Reset from low voltage reset
WDT	System Reset from watch dog timer

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Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC2.L	1BH	00	R/W	*7	*6	*5	*4	*3	*2	*1	-	System miscellanea register
MISC2.H	1BH	00	R/W	*15	*14	*13	*12	*11	*10	*9	*8	

MISC2 register	**Definition**
INT_MASK_EN (*15)	Masked Interrupt Enable bit
SPI_NEW_MODE (*14)	New SPI Control Mode Enable bit
FIRQ_PIN_INV (*13)	FIRQ External Input Pin Inverse
FIRQ_PIN_SEL (*12)	FIRQ External Input Pin Select: 0(PA4), 1(PB4)
EXTTIMER2_PIN_INV (*11)	Timer 2 External Input Pin Inverse
EXTTIMER2_PIN_SEL (*10)	Timer 2 External Input Pin Select: 0(PB0), 1(PC2)
EXTTIMER1_PIN_INV (*9)	Timer 1 External Input Pin Inverse
EXTTIMER1_PIN_SEL (*8)	Timer 1 External Input Pin Select: 0(PA5), 1(PB5)
EXTINT1_PIN_INV (*7)	External Interrupt 1 Input Pin Inverse
EXTINT1_PIN_SEL (*6)	External Interrupt 1 Pin Select: 0(PA7), 1(PB7)
EXTINT0_PIN_INV (*5)	External Interrupt 0 Input Pin Inverse
EXTINT0_PIN_SEL (*4)	External Interrupt 0 Pin Select: 0(PA6), 1(PB6)
PWMIO_MODE (*3)	PWM PAD I/O Mode
PWMNIO_EN (*2)	PWMN PAD I/O Mode Enable bit
PWMPIO_EN (*1)	PWMP PAD I/O Mode Enable bit

◆ Virtual Programming IO

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
VIO_IX	1EH	XX	W	IOPIX7	IOPIX6	IOPIX5	IOPIX4	IOPIX3	IOPIX2	IOPIX1	IOPIX0	Programming IO Port index
VIO_DATA	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

Table 5.2 Virtual Programming IO

The operation steps of these group register, first select virtual IO port index then write data to programming IO port.

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	XX	W	Timer0[15:0]								Timer1
Timer2	01H	XX	W	Timer1[15:0]								Timer2
RTCTimer	02H	00	W	-	-	-	-	-	DIVSEL2	DIVSEL1	DIVSEL0	RTC RC-oscillator divider
Timer_ Config	03H	00	W			Timer2_Trig_SEL				Timer1_Trig_SEL		Timer Trigger Source Configuration
TOUCH_ CTL	04H	00	RW	TOUCH_CONTROL(see 7.7.5)								Touch control register
TOUCH_ DAT	05H	00	RW	TOUCH_DATA (see 7.7.5)								Touch data register
FIRQ_ Config.L	06H	00	W	*8	*7	*6	*5	*4	*3	*2	*1	FIRQ Configuration Low Byte
FIRQ_ Config.H	06H	00	W	-	-	-	-	*12	*11	*10	*9	FIRQ Configuration High Btye

Timer_Config	**Definition**
Timer1_Trig_SEL[0]	Timer 1 External Trigger Enable bit
Timer1_Trig_SEL[1]	Timer 1 External Trigger Edge Select: 0(Rising), 1(Falling)
Timer2_Trig_SEL[0]	Timer 2 External Trigger Enable bit
Timer2_Trig_SEL[1]	Timer 2 External Trigger Edge Select: 0(Rising), 1(Falling)

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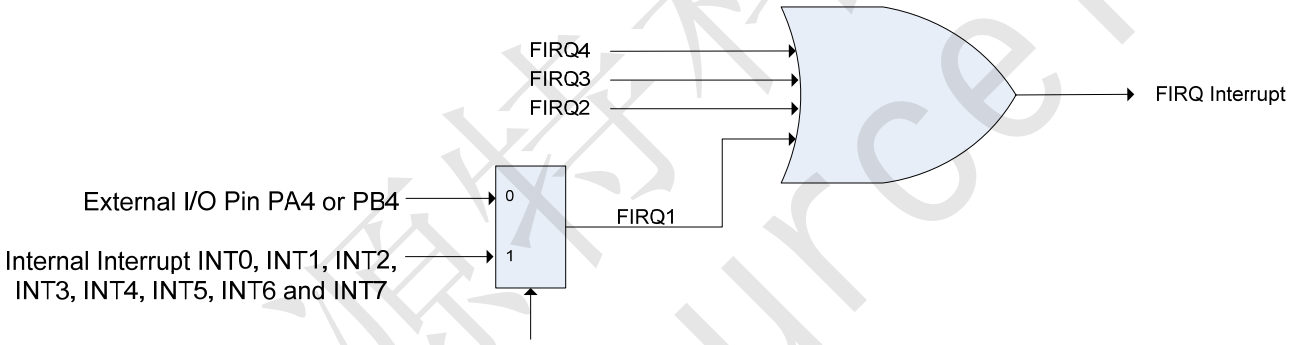
FIRQ_Config	Definition
FIRQ_Config11 (*12)	INT5 to FIRQ4 Enable bit
FIRQ_Config10 (*11)	INT4 to FIRQ3 Enable bit
FIRQ_Config9 (*10)	INT0 to FIRQ2 Enable bit
FIRQ_Config8 (*9)	FIRQ1 Trigger Source Select: 0(External I/O Pin PA4 or PB4), 1(Internal Interrupt INT0, INT1, INT2, INT3, INT4, INT5, INT6 and INT7)
FIRQ_Config7 (*8)	INT7 to FIRQ1 Enable bit
FIRQ_Config6 (*7)	INT6 to FIRQ1 Enable bit
FIRQ_Config5 (*6)	INT5 to FIRQ1 Enable bit
FIRQ_Config4 (*5)	INT4 to FIRQ1 Enable bit
FIRQ_Config3 (*4)	INT3 to FIRQ1 Enable bit
FIRQ_Config2 (*3)	INT2 to FIRQ1 Enable bit
FIRQ_Config1 (*2)	INT1 to FIRQ1 Enable bit
FIRQ_Config0 (*1)	INT0 to FIRQ1 Enable bit

Notice: If External interrupt 0(EXTINT0) or External interrupt 1(EXTINT1) or External interrupt 2(EXTINT2) is configured to FIRQ, Double edge trigger of corresponsive external interrupt will be disable.



FIRQ Source Configuration Diagram

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5.3 PC Stack

The PC STACK is TxP16 special embedded memory used to save (PC+1) value, which is composed with 16-level.

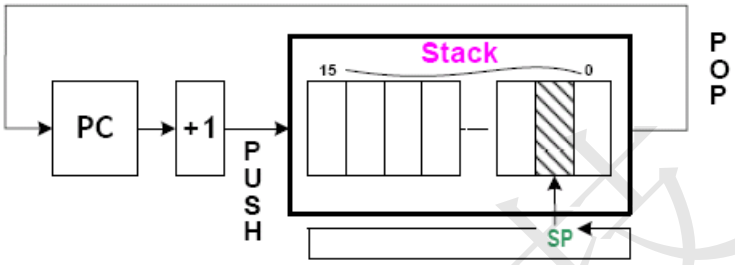

Figure 5.3 PC Stack Structure

Stack's top value is indexed by stack pointer (SP) register. When CALL instruction is executed, then the (PC+1) will PUSH onto stack addressing by SP and it will auto decrement. At the end of subroutine when RETS instruction is executed the SP will auto increment and stack content of pointer by SP will POP into PC.

The contents of STACK and SP are neither readable nor writeable by instruction. The SP is initialized to “0” after RESET.

5.4 Interrupt

5.4.1 Interrupt Vector Table

The Interrupt Vector Table is TxP16 special embedded memory, which is composed with 9-level of FIFO, used to store the index of interrupt service routine (ISR) address. User can access Interrupt Vector Table by read/write IntVect I/O register.

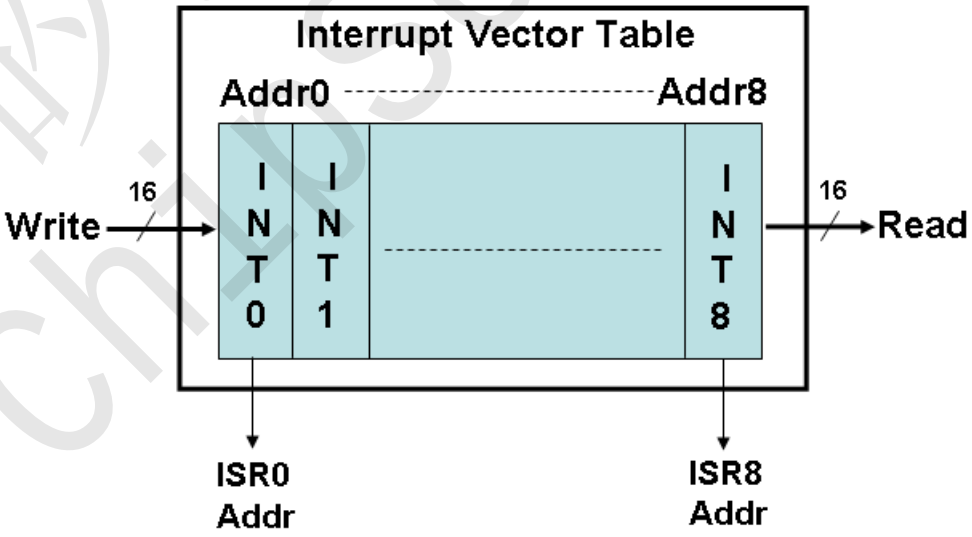

Figure 5.4 Interrupt Vector Structure

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5.4.2 Interrupt Controller

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS.L	00H	20	R/W	INTEN			AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR				UART_EN	SPI_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Int Enable
INTENA.H	01H	00	R/W	-	-	-	-	-	-	-	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Int Request
INTREQ.H	02H	00	R/W	-	-	-	-	-	-	-	Req8	
INTMASK.L	0FH	00	R/W	Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0	Interrupt Mask
INTMASK.H	0FH	00	R/W	-	-	-	-	-	-	-	Mask8	

This chip provides several interrupt sources, including internal Audio PWM, Timer1, Timer2, RTC Timer, UART, SPI master, ADC, Touch and 3 external ExtINT0, ExtINT1, ExtINT2 interrupts, and FIRQ interrupt. More details control will describe as follows:

Interrupt Source	Interrupt Vector	Priority
Audio PWM Timer / ExtINT2	0H	INT0_IRQ
Timer1	1H	INT1_IRQ
Timer2	2H	INT2_IRQ
RTC Timer	3H	INT3_IRQ
ExtINT0 / ADC	4H	INT4_IRQ
ExtINT1 / UART	5H	INT5_IRQ
SPI Master	6H	INT6_IRQ
TOUCH	7H	INT7_IRQ
FIRQ	8H	INT8_IRQ

Table 5.2 CST16P161A Interrupt Sources

(a) Global interrupt enable(INTEN)

The global interrupt INTEN controls the enable/disable of all interrupts. When INTEN is cleared to “0”, all interrupts are disabled. When INTEN is set to “1”, all interrupts are enabled (but still dependent on value of INTENA register). The INTEN is initialized to “”0” after power on

(b) Interrupt enable (INTENA)

The interrupt enable ENA0, ENA1, ENA2, ENA3, ENA4, ENA5, ENA6, ENA7, ENA8 are shown in above. An interrupt is allowed when these control bit are set to “1”, and interrupt is inhibit when these control bit are cleared to “0”. They are all initialized to “0” after power on.

(c) Interrupt request (INTREQ)

If an interrupt **raising edge** request is generated, the related interrupt request bit is set to “1” by hardware and waits for interrupt accept. INTREQ can be cleared to “0” by software. Hardware will not clear this bit. INTREQ are all initialized to “0” after power on.

(d) Interrupt mask (INTMASK)

The interrupt can be masked by setting Mask[8:0] interrupt mask register as above. Each interrupt source in the system can be masked individually.

(e)Configurable FIRQ Interrupt Source

FIRQ interrupt source can be programmable. User can assign any interrupt source as FIRQ interrupt source. For Example, user can assign SPI Master interrupt source to FIRQ(INT8_IRQ), and then SPI Master interrupt

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priority will be changed to highest level.

(f) Interrupt Priority

INT8_IRQ (highest) > INT0_IRQ > INT1_IRQ > INT2_IRQ > INT3_IRQ > INT4_IRQ > INT5_IRQ > INT6_IRQ > INT7_IRQ(lowest).

Interrupt Source	Interrupt Vector	Priority(default)
Audio PWM Timer / ExtINT2	0H	INT0_IRQ
Timer1	1H	INT1_IRQ
Timer2	2H	INT2_IRQ
RTC Timer	3H	INT3_IRQ
ExtINT0 / ADC	4H	INT4_IRQ
ExtINT1 / UART	5H	INT5_IRQ
SPI Master	6H	INT6_IRQ
TOUCH	7H	INT7_IRQ (lowest)
FIRQ(Fast Interrupt Request)	8H	INT8_IRQ(highest)

Notice: If External interrupt 0(EXTINT0) or External interrupt 1(EXTINT1) or External interrupt 2(EXTINT2) is configured to FIRQ, Double edge trigger of corresponsive external interrupt will be disable.

5.4.3 Interrupt Processing

When any interrupt request(INTREQ) is generated, the acceptance of interrupt is decided by the interrupt enable(ENA) and global interrupt enable(INTEN). If the interrupt enable and global interrupt enable related bit are set to “1”, that interrupt will be accepted on the next clock. These following procedures will automatically be done in one clock cycle by hardware showing below:

(1) Program Counter(PC), PCH, AR and FLAG will be stored in special hardware registers.

(2) PC will be set to the corresponding interrupt entry address by refer to interrupt vector table.

(3) The global interrupt enable (INTEN) is cleared to “0”, which avoids the nest interrupt happened.

When interrupt service routine was finished, an RETI instruction will perform the procedures by hardware showing as follows:

(1) Restore the stored PC, PCH, AR and FLAG.

(2) The global interrupt enable (INTEN) is set to “1”, which allows to accept the subsequent interrupt.

Before executing RETI instruction, the corresponding interrupt request (INTREQ) bit must be cleared to “0” by software. If the request bit is not cleared, the same interrupt will be accepted again.

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5.5 MAC (16-bit X 16-bit Multiplier and Accumulator)

A 16 bit x 16 bit MAC is provided for digital signal processing. The core of MAC operation is multiply MX&MY with 2'S complement operand and accumulation previous 40-bit MF then rounding store result in the 40-bit MR register. The basic MAC architecture is shown as Figure 5.5.

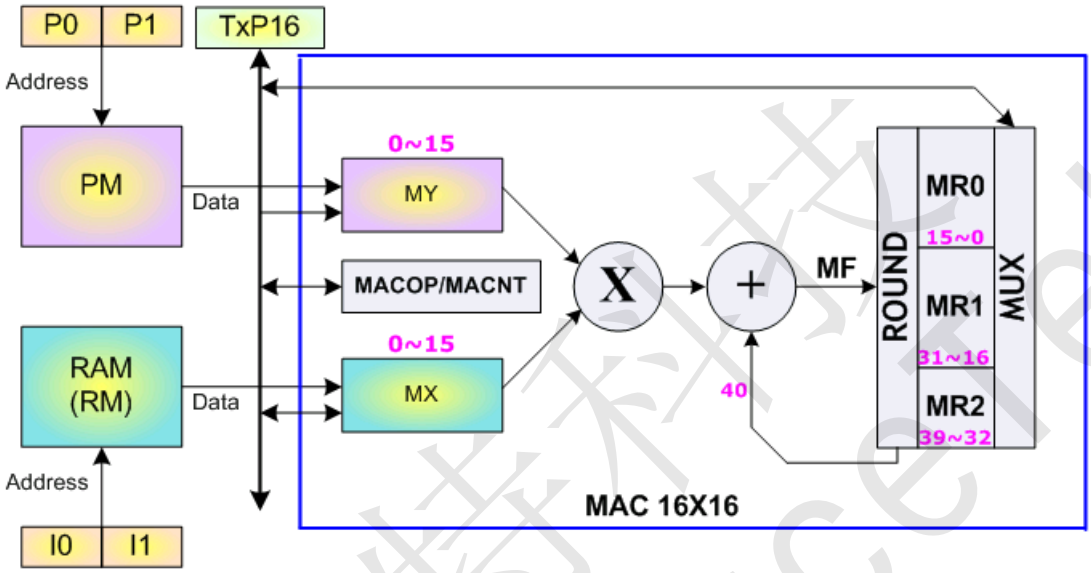

Figure 5.5 MAC Architecture

Define MAC module registers:

MX: MAC input 16-bit X register

MR: Multiplier or MAC result 40-bit register

MACOP: MAC operation define register

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup

MACNT: MAC equation loop counter, max to 255

Basically, multiplier operates equation:

MR = MX*MY(SU) → MX: signed, MY: unsigned

Permission MY is AR or immediate value (-128~127), MX and MY are signed or unsigned assign by MACOP. So, actual multiplier instruction likes this:

MR = MX*AR or MR = MX*56

The operation of MAC equation is:

MR = MR + (MX*MY(SU))<<RND, MX=RM[I0++], MY=PM[P1--]

The means of equation is signed MX multiply unsigned MY the result value shift left RND bits and add previous MR then write back to MR.

Simultaneously, load new value to MX fixed from RM[index operation]

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MY fixed from PM[pointer operation]

Therefore, MAC array operation like this:

```
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
                .
                .                                          Successive 64 times
                .
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
```

Actual just one line of instruction present in assembly coding like this:

MACNT = 63

This is very benefit for reducing code size. Of curse, we need setup MACOP register previous; at this example is like this;

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup
			0	1	1	1	0	0	0	0	

Note: Successive MAC operation will cause MCU interrupt disable.

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6. CST16P161A Memory Configuration

6.1 Internal Program/Parameter Memory

TxP16 consider both instruction and data ROM are the same as program ROM(PM), so it's very flexible and efficient for instruction and data memory allocation in PM. On the logical PM space is organized into 12kx16-bit which is addressed by memory address generator unit (MAG). Actual PM is separated into two parts including read only 12K OTP ROM(Page0) and write available 16-word SRAM(Page1). User can dynamic download program/data to page1 for MCU get more flexible operation. More details control will describe as follows:

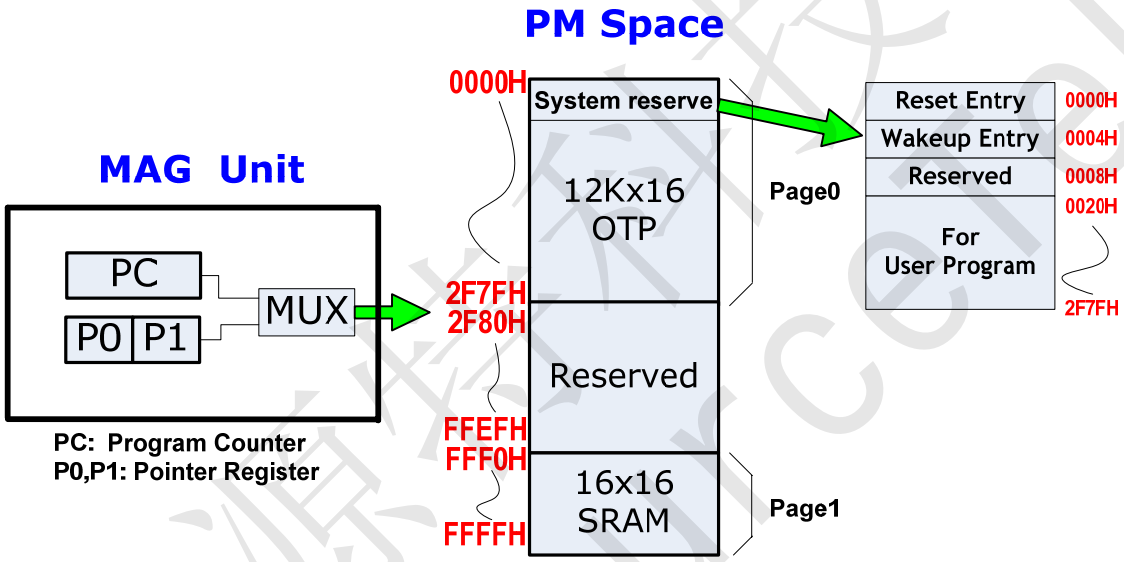

Figure 6.1 CST16P161A PM block diagram

When TxP16 executed an instruction, the PM address is generated from PC register. Similarity, when it access a word data, the PM address is composed with 16-bit from P0 or P1. System will auto adjust execute target space when program context switch between page0 and page1.

6.2 Internal Data Working SRAM

The internal data working ram space is totally 3072X16-bit that named as RM. Addressing ranged from 0000H through 08FFH, which is generated by Data Address Generator Unit (DAG). Note: Index register (I0,I1,BP) are 16-bit width, but RM address line is only 12-bit width(0~4095); therefore, RM address will be warping when index value exceed 4095.

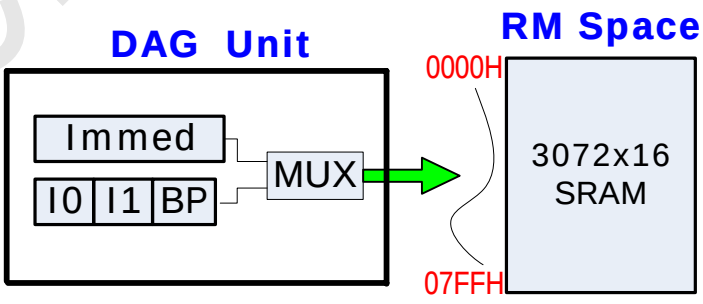

Figure 6.2 CST16P161A RM block diagram

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6.2 Data Stack

A Last In First Out (LIFO) STACK is implementation for temporary data storage in RM memory. Generally, Data Stack is start-up at the bottom of RM, so BP is usually set to 0x07FF.

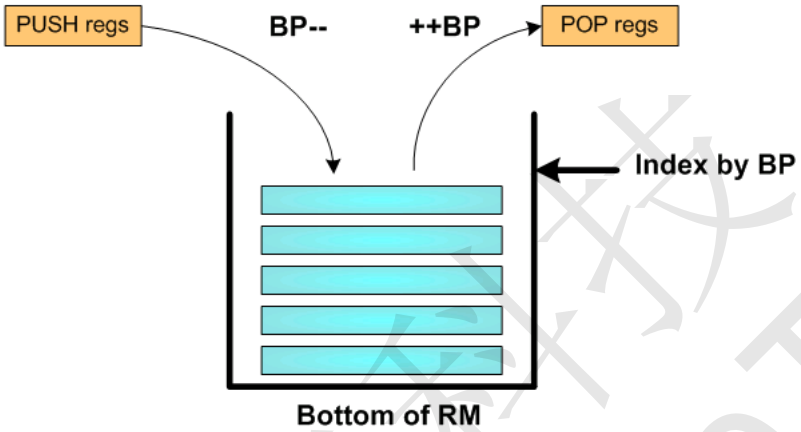

Figure 6.3 Data Stack Structure

Data Stack's top value is indexed by base pointer (BP) register. When PUSH instruction is executed, the “regs” will PUSH onto stack which address by BP and it will auto decrement. If POP instruction is performed, the BP will auto increment and stack content of pointed by BP will POP into “regs”.

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7. CST16P161A Peripherals

7.1 Programmable Timers

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS.L	00H	20	R/W	INTEN			AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR				UART_EN	SPI_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Int Enable
INTENA.H	01H	00	R/W	-	-	-	-	-	-	-	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
INTREQ.H	02H	00	R/W	-	-	-	-	-	-	-	Req8	

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	XX	W	Timer0[15:0]								Timer1
Timer2	01H	XX	W	Timer1[15:0]								Timer2
RTCTimer	02H	00	W	-	-	-	-	-	DIVSEL2	DIVSEL1	DIVSEL0	RTC RC-oscillator divider
Timer_Config	03H	00	W			Timer2_Trig_SEL				Timer1_Trig_SEL		Timer Trigger Source Configuration

7.1.1 PWM Timer

PWM timer is fixed generate 32kHz interrupt request when INTENA0 bit is turned on, *If Auto FIFO_EN is setting the interrupt request rate = Ft/FIFO_Length.*

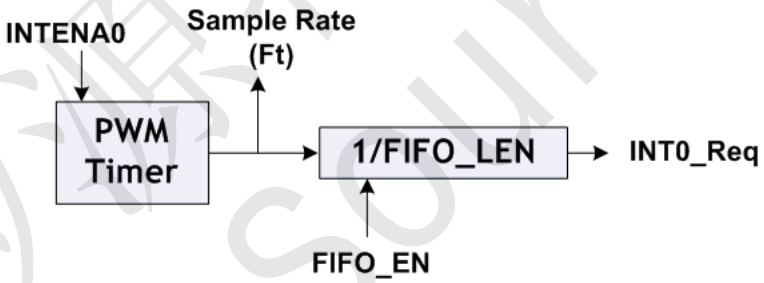

Figure 7.1 PWM Timer Structure

7.1.2 Timer1 & Timer2

The clock source of Timer1&Timer2 comes from fixed 32.768Mhz, It contains 16-bit write-only counter register. If Timer enable correspond with the INTENA bit is turned on then counting to time out, an interrupt request will be generated. At the same time, TnC in Eq.(7.1.1) will be reloaded into Timer register and up-count again. If the global interrupt enable, an interrupt signal is generated at the next clock.

Int1_Req / Int2_Req = 32.768MHz / (TnC+1) or

Int1_Req / Int2_Req = External Clock Input / (TnC+1)

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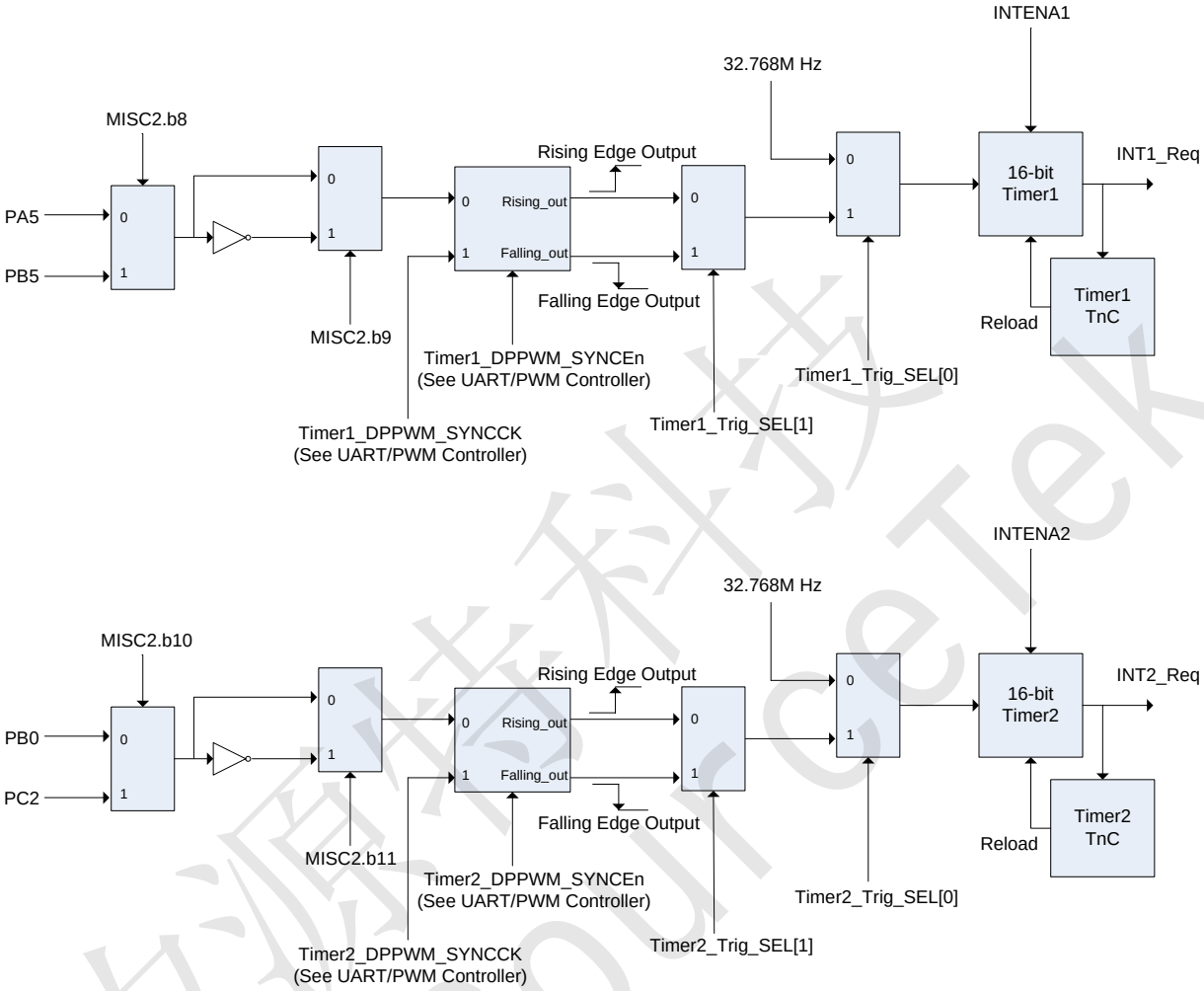

Figure 7.2 Timer1&Timer2 Structure

7.1.3 RTC Timer

The RTC Timer input frequency can select 32K XTAL(32768Hz) or Low power RC oscillator 32768Hz ± 2% (LP32K) by option. It contains 12-bit counter register. RTC generates interrupt request or wake-up MCU when in halt mode or interrupt in normal mode. The wake-up function can be disabled by option, default wake-up function is enabled and INT3_Req is set to high after 2ms when reset occurred. The counter of divider will be reset once while going into halt mode, and MCU will be wake-up or interrupt after 2ms if DIVSEL2,DIVSEL1,DIVSEL0=000.

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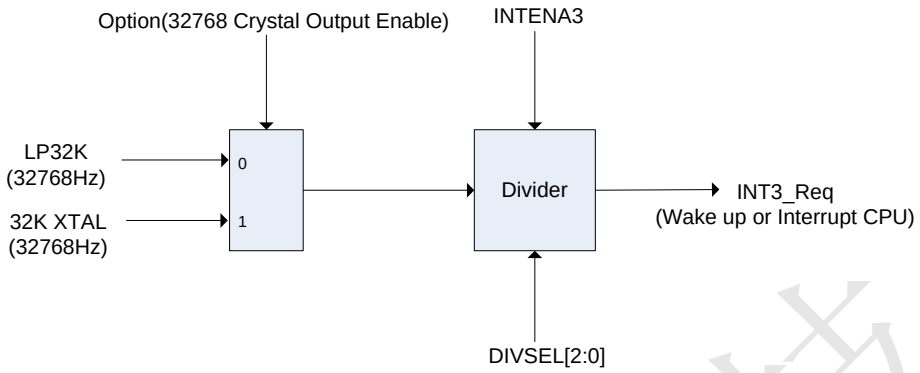

DIVSEL2	DIVSEL1	DIVSEL0	Period
0	0	0	2ms
0	0	1	4ms
0	1	0	8ms
0	1	1	128ms
1	0	0	0.0625 ms
1	0	1	0.125 ms
1	1	0	0.25ms
1	1	1	1ms

Figure 7.3 RTC Timer Structure

Notice: IDE Tool has embedded a demo code to illustrate RTC Timer auto-calibration function.

7.2 General Purpose I/O Ports

The CST16P161A provides 3 I/O ports for user application. There are four I/O port, PA0~PA7, PB0~PB7, and PC0~PC7. The input/output bits programmable by IOC control register respectively. PA0~PA7, PB0~PB7 wake-up function enable or disable by programmed option, and PA7~ PA6 is external interrupt pin. The pull-down 50k resistor of each pin can be programmed by option. The basic I/O schematic is showed in Figure 7.4.

These totally 24 I/O pins work not only just a general input/output port function but also can configure to UART , Serial Flash/ROM interface. For more detail please refer to relative section.

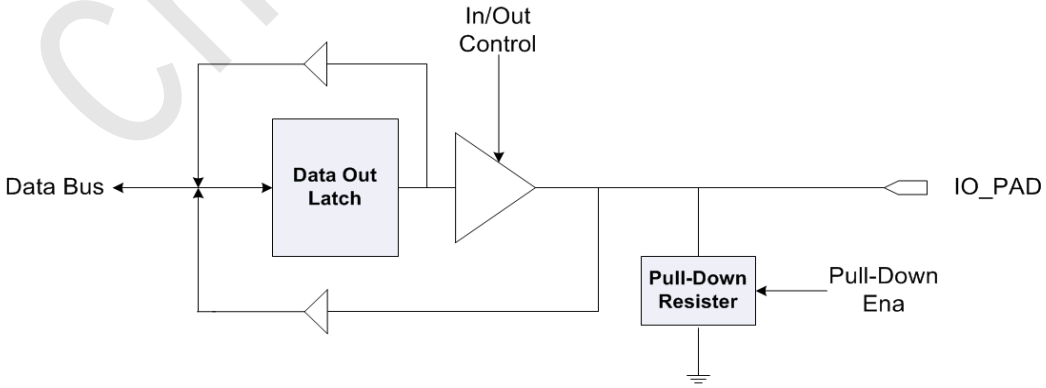

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Figure 7.4 Basic I/O Configuration

PB0,PB1 support two edge modes for wake-up function are rising and falling edge trigger. The rising and falling edge trigger is selected by option.

The PortC0~PortC7 also provides 4 comparators configuration for user application that each comparator enable or disable by programmed option.

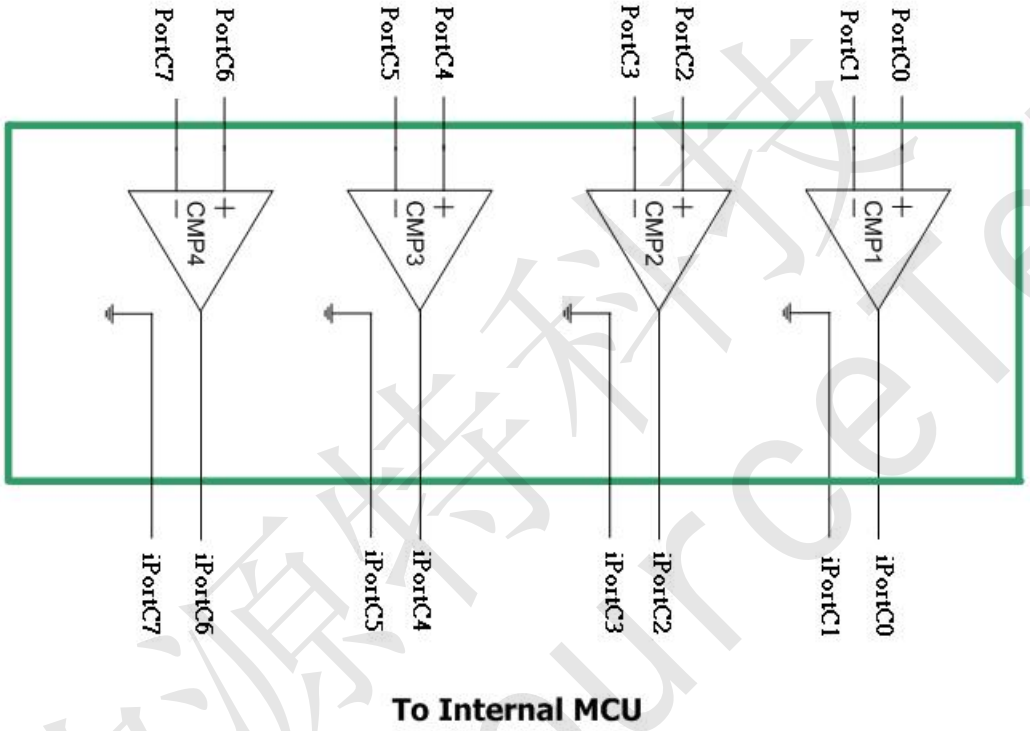

Figure 7.5 Comparator Configuration

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7.3 Extension Device

CST16P161A built-in special hardwires for external device connection capability are listed below:

7.3.1 SPI Controller

In order to enable SPI Controller interface, user should set STATUS.b8 = 1 before SPI Controller operation.

7.3.1.1 Features

- Designed for read-only and read/write data
- Support MXIC Serial Flash
- Serial clock rate: 32.768 MHz / 16.384 MHz / 13.107 MHz / 10.922 MHz / 8.192 MHz / 4.096 MHz
- Built in 4x16 bits data buffer

I/O Port	SPI interface	Direction	Description
PortA.0	SO	I	Serial Data output to MCU
PortA.1	SI	O	Serial Data input from MCU
PortA.2	SCK	O	Serial Clock
PortA.3	CS	O	Chip Select(free assign by user)

7.3.1.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	0DH	01	W	-	CLR	RCV	SEND	Total Send/Receive Byte				Control Register Low Byte
CTRL_W.H	0DH	00	W	Mode	CKSEL			ICS	-	-	-	Control Register High Byte
CTRL_R.L	0DH	00	R	DATOK	CLR	RCV	SEND	Total Send/Receive Byte				Read Status Low Byte
CTRL_R.H	0DH	00	R	Mode	CKSEL			ICS	-	BFINX1	BFINX0	Read Status High Byte

Total Send/Receive Byte: Total byte number of sending or receiving.

ICS: Internal SPI command select enable.

SEND: Trigger sending data.

RCV: Trigger receiving data.

CLR: Clear control flag.

CKSEL: (000: 32.768MHz), (001: 16.384MHz), (010: 13.107 MHz), (011: 10.922 MHz), (100: 8.192 MHz), (101: 4.096 MHz).

Mode: (0:Posedge latch data), (1:Negedge latch data).

DATOK: Indicate transmit/receive data O.K.

BFINX [1:0]: Indicate which data buffer is accessed by CPU.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
DATA_W	0EH	XX	W	DATA[15:0]								Write Transmission Data Value
DATA_R	0EH	XX	R	DATA[15:0]								Read Received Data Value

DATA [15:0]: Transmit/Receive Data Value

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Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC2.L	1CH	00	R/W	*8	*7	*6	*5	*4	*3	*2	*1	System miscellanea register
MISC2.H	1CH	00	R/W	*16	*15	*14	*13	*12	*11	*10	*9	

MISC2 register	**Definition**
SPI_NEW_MODE (*15)	New SPI Control Mode Enable bit

SPI_NEW_MODE: 1-> Enable NEW SPI Control Mode.

1. If SPI_NEW_MODE is set to high, improved control mode is choose.
2. If SPI_NEW_MODE is set to low, old control mode is choose.

Improved control mode is that user can access SPI data, don't need to polling DATOK.

Notice that more detail SPI operation sequence, please ref. Appendix.

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7.3.2 UART/PWM Controller

In order to enable UART/PWM Controller interface, user should set STATUS.b9 = 1 for UART/PWM Controller before UART/PWM controller operation.

7.3.2.1 Features

- Baud Rate up to 115200
- Even, odd, or no-parity bit generation and detection
- 1-stop bit generation
- IR carrier with pulse width adjustment
- 1 channel PWM

UART I/O Port	UART interface	Direction	Description
PortB.2	SIN(RX)	I	UART Data input to MCU
PortB.3 / PWMP	SOUT(TX)	O	UART Data output from MCU

PWM I/O Port	PWM interface	Direction	Description
PortB.0 / PWMP	PWM1P	O	PWM1P Output
PortB.1 / PWMN	PWM1N	O	PWM1N Output

7.3.2.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	12H	XX	W	Set_ Pulse_ Width	UART_ FUN_ EN	IR_FUN _EN	Set_ Baud_ Rate	user_bit	Set_ Parity	RXIRQ En	TXIRQE n	Control Register Low Byte
CTRL_W.H	12H	XX	W	-	-	-	-	-	-	uart_pin _type	Set_ Carrier_ Freq	Control Register High Byte
CTRL_R.L	12H	00	R	Set_ Pulse_ Width	UART_ FUN_ EN	IR_FUN _EN	Set_ Baud_ Rate	user_bit	Set_ Parity	RXIRQ En	TXIRQE n	Read Status Low Byte
CTRL_R.H	12H	00	R	RxERR OR	TX_ BufEmp ty	RX_ DataRe ady	ParityEr r	Overrun Err	TXINT_ or_RXI NT	uart_pin _type	Set_ Carrier_ Freq	Read Status High Byte

TXIRQEn : TX IRQ Enable

RXIRQEn : RX IRQ Enable

Set_Parity : Set UART Parity

user_bit : User Define Bit

Set_Baud_Rate : Set Baud Rate

IR_FUN_EN : IR Function Enable

UART_FUN_EN : UART Function Enable

Set_Pulse_Width : Set pulse width for IR carrier and PWM1P

Set_Carrier_Freq : Set Carrier Frequency

uart_pin_type : (0: SOUT IO Pin is PortB.3), (1: SOUT IO Pin is PWMP) *Note: uart_pin_type will active PWM PAD.*

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TXINT_or_RXINT: (0: TX Interrupt Happen), (1: RX Interrupt Happen).

OverrunErr : RX Overrun Error

ParityErr : Parity Error

RX_DataReady : RX Data Ready Flag

TX_BufEmpty: TX Data Buffer Empty Flag

RxERROR : Receive Data(RX) Miss STOP Bit

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
DATA_W.L	13H	XX	W	Write_DATA_Buffer[7:0]								Write Data Buffer Low Byte
DATA_W.H	13H	XX	W	Write_DATA_Buffer[15:8]								Write Data Buffer High Byte
DATA_R.L	13H	00	R	RX_DATA[7:0]								Read Received Data Low Byte
DATA_R.H	13H	00	R	0	0	0	0	0	0	0	0	Read Received Data High Byte

OPTION	Write_DATA_Buffer[15:0]															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Set_Parity = 1	-	Carrier_ Enable	Carrier_ Mode[1:0]		-	-	-	-	-	-	-	SE	-	-	-	EN
Set_Baud_Rate = 1	-	-	-	-	Divisor[11:0]											
Set_Carrier_Freq = 1	OS1	-	-	FCarrier[12:0]												
Set_Pulse_Width = 1	-	-	Set_ P1Width_ sync	PWidth[12:0]												
(Set_Baud_Rate = 0) & (Set_Carrier_Freq=0) & (Set_Pulse_Width=0)	-	-	-	-	-	-	-	-	TX_DATA[7:0]							

TX_DATA[7:0] : Transmit Data Value

RX_DATA[7:0] : Receive Data Value

EN : Parity Enable

SE : (0: Odd Parity), (1: Even Parity)

Carrier_Enable : IR Carrier Enable

OS1 : PWM1 One shut : (1:pwm1 one shut enable), (0:pwm1 one shut disable)

Set_P1Width_sync : The PWM1N information are synchronized with PWM1P, when this bit set zero. The information include pulse width.

Baud Rate Table: (Set_Baud_Rate = 1)

Baud Rate	Divisor (Decimal)	Baud Rate	Divisor (Decimal)
50	2304	3600	32
75	1536	4800	24
110	1047	7200	16
134.5	857	9600	12
150	768	19200	6
300	384	38400	3
600	192	57600	2
1200	96	115200	1
1800	64		
2000	58		
2400	48		

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IR / PWM1 Carrier Freq Formula : (Set_Carrier_Freq = 1)

IR / PWM1 Carrier Freq = 1.8432MHz / (FCarrier[12:0] x 2)

For example : FCarrier[12:0] = 0x0018 IR / PWM1 Carrier Freq = 38400 Hz

PWidth[12:0]: IR / PWM1 carrier pulse width can be adjusted by PWidth[12:0] register.

Pulse Width = (PWidth[12:0]+1) times of 65.536MHz clock cycles.

Carrier_Mode[0] : (0: Transmit Waveform Modulation by user_bit register), (1: Transmit Waveform Modulation by UART Data).

Carrier_Mode[1] : (0: Non-Invert Transmit Waveform), (1: Invert Transmit Waveform).

Note: Hardware of IR function shared with PWM1 function. The operation of PWM1 function is same as user_bit mode of IR function.

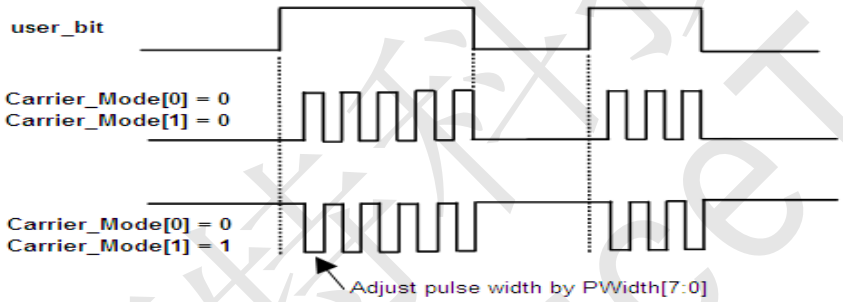

Figure 7.6 IR waveform of user_bit mode (Carrier_Mode[0]=0)

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7.4 Audio Output

The three configurations of audio output form in CST16P161A system are stereo 16-bit PWM, stereo 15-bit PWM and mono 16-bit PWM. The kind of solution is determined by user's application. Notice that each time there is only one type of PWM can be specified, which assign by option. The PWM PIN configuration shows as below:

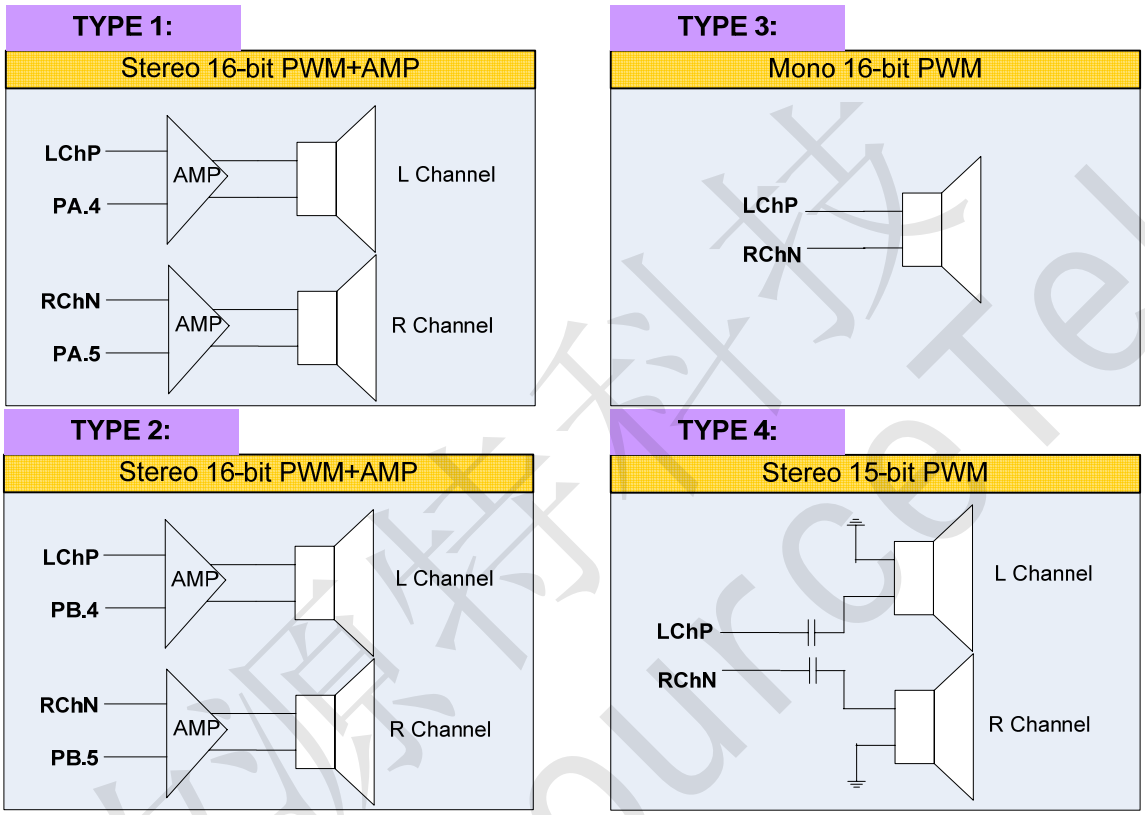

Figure 7.7 PWM output configuration

7.4.1 Stereo PWM Output

Two 16-bit resolution of PWM converters are built-in CST16P161A for stereo audio application. In order to get more output power driving, which require external amplifier for stereo output pin.

Additionally, two 15-bit of PWM amplifiers(Type4) are also built-in CST16P161A for stereo audio application.

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	B13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
DACL	16H	XX	W	DACL [15:0]								DAC Audio L Channel
DACR	17H	XX	W	DACR [15:0]								DAC Audio R Channel

7.4.2 Mono PWM Output

A 16-bit of PWM amplifiers is built-in(Type3) CST16P161A system. This amplifier can be used to direct drive 8 ohm speaker without any external circuit.

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
DACL	16H	XX	W	DACL [15:0]								16-bit PWM Channel

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7.4.3 Mono DAC Output

Two 16-bit of digital-to-analog convert are built-in CST16P161A for mono audio application. In order to get more output power driving, which require external amplifier for audio output pin **PWMP.**

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	B13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
DACL	16H	XX	W	DACL [15:0]								DAC Audio L Channel

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7.5 Auto-FIFO

The Auto-FIFO allows user transfer base on 4-level of data to PWM D/A. In some case of frame base applications that data transfer is more efficient than sample base. It is advantageous to decrease number of context switch between main program and interrupt service routine (ISR). The FIFO structure reveal as below:

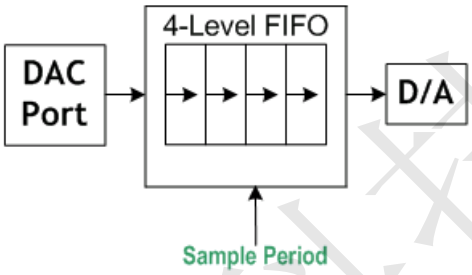

Figure 7.8 Auto FIFO Structure

An interrupt is generated when an entire 4-level FIFO is transfer completed (D\A FIFO buffer is empty), then interrupt service routine should re-load 4-level data to FIFO at ones during 32K sample period. The FIFO will automatically shift-out data to PWM D/A at each sample period.

Note: Auto-FIFO is enable/disable by option setup up.

Note: Emulator doesn't support PWM Mute function for emulation, user need to notice this difference between Emulator and Real Chip.

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7.6 8channel / 10 bits signed ADC

7.6.1 Features

- 8 external I/O input Channels
- 10-bit Signed ADC
- Up to 71.2K samples per second (@ACQT = 4*TAD, ADC clock = 1Mhz)
- Programmable acquisition time
- ADC start conversion by S/W, Audio PWM, Timer, RTC or External I/O pin
- Built in 4x10 bits ADC data buffer

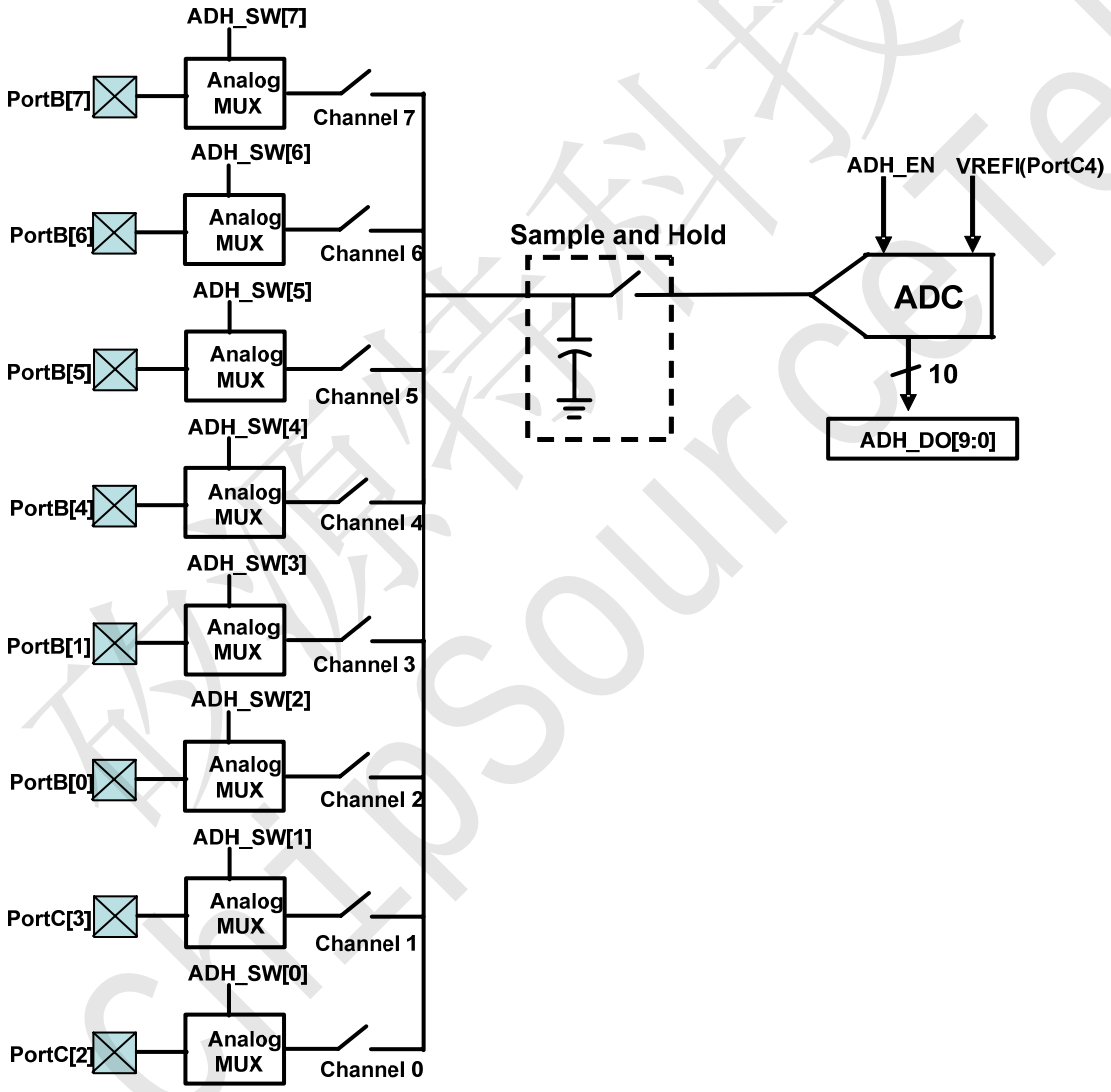

Figure 7.8 8-Channels / 10-bits ADC Structure Diagram

Note: If user need more precise ADC for application, user can use PortC4 as voltage-reference input(VREFI) of ADC. Independent voltage-reference input pin can improve ADC precision.

Note: Enable ADC verf input at program, PortC4 is as ADC voltage-reference input(VREFI), not as I/O pin.

*** The decouple capacitor (10uF) must be as near as possible to VCC and VSS.*

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7.6.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG0.L	40H	00	R/W	0	0	ACQT[1:0]		0	0	0	ADCS	10-bit ADC control0
ADL_CFG0.H	40H	00	R/W	ADH_EN	ADH_IEN	VREFI_EN	SIGN_EN	0	TRGSRC [2:0]			

ADH_EN: 10-bit signed ADC enable bit

ADH_IEN: ADC interrupt enable bit

VREFI_EN: ADC VREF input(PC4) enable bit

(When VREFI_EN is set, PortC4 must be connected 20~100ohm resistor to VCC and 47uF capacitor to AVSS)

SIGN_EN: Sign ADC Data output enable bit. (*sign ADC Data = unsign ADC Data ^ 10'h200*)

ADCS: ADC clock select bit. 0 = 512Khz 1 = 1Mhz

TRGSRC[2:0] : Select trigger source

000 = software trigger 001 = Audio PWM 010 = Timer1 011 = Timer2

100 = RTC Timer 101 = PortA[6] 11X = PortB[4]

ACQT[1:0] : A/D acquisition time select bits

00 = 2 TAD 01 = 4 TAD(default) 10 = 8 TAD 11 = 16 TAD

Note: If ADH_EN is not set to high, ADH_CFG1 can not be written.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG1.L	41H	00	R/W	ADH_SW[7:0]								10-bit ADC control1
ADL_CFG1.H	41H	00	R/W	SWTRG	ADH_SW[14:8]							

SWTRG : Software Trigger

1 = Setting this bit starts the A/D conversion cycle.

This bit is automatically cleared by hardware when A/D conversion has completed.

0 = A/D conversion is completed

ADH_SW[14:0] : These PortB[7:4], PortB[1:0] and PortC[3:2] pins associated with the 10-bit A/D Converter can individually be configured as an analog input or digital I/O using the ADH_SW[7:0] registers.

ADH_SW[14]: 1 = VDD (LDO 2.8V)

ADH_SW[13]: 1 = VSS (Chip Ground)

ADH_SW[12]: 1 = VREF

ADH_SW[11]: 1 = N/C

ADH_SW[10]: 1 = N/C

ADH_SW[9]: 1 = BGO (Bandgap 1.2V)

ADH_SW[8]: 1 = Microphone amplifier analog input (Refer to Sector 8.4)

ADH_SW[7]: 1 = PortB[7] is channel 7 analog input, 0 = PortB[7] is digital I/O

ADH_SW[6]: 1 = PortB[6] is channel 6 analog input, 0 = PortB[6] is digital I/O

ADH_SW[5]: 1 = PortB[5] is channel 5 analog input, 0 = PortB[5] is digital I/O

ADH_SW[4]: 1 = PortB[4] is channel 4 analog input, 0 = PortB[4] is digital I/O

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ADH_SW[3]: 1 = PortB[1] is channel 3 analog input, 0 = PortB[1] is digital I/O

ADH_SW[2]: 1 = PortB[0] is channel 2 analog input, 0 = PortB[0] is digital I/O

ADH_SW[1]: 1 = PortC[3] is channel 1 analog input, 0 = PortC[3] is digital I/O

ADH_SW[0]: 1 = PortC[2] is channel 0 analog input, 0 = PortC[2] is digital I/O

Note: If user need to enable more A/D channels than one, user should enable ADC interrupt in order to read A/D conversion data of more channels. When some one channel is converted completely, it will generate an interrupt to CPU. Every active channel is converted sequentially.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG2.L	42H	00	R/W	-	-	-	*5	*4	*3	*2	*1	10-bit ADC control0
ADL_CFG2.H	42H	00	R/W	-	-	-	-	-	-	-	-	

ADC_BUF_SIZE_SEL(*1): ADC Buffer Size Select (1-> Four Level, 0-> Two Level)

ADC_ PINGPONG_EN(*2): ADC Ping-Pong Buffer Enable bit. If this bit is enabled, ADC Buffer Size will be half of original buffer size.

ADC_BUF_EN(*3): ADC Data Buffer Function Enable bit. If this bit is disabled, ADC buffer size will be zero.

RD_ADC_MODE2(*4): If this bit is enabled, next adc channel will not be converted until user read current adc data.

CLR_BUF_SEL(*5): Clear internal ADC data buffer index pointer.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_DO.L	44H	00	R	ADH_DO[1:0]		0	0	0	0	0	0	10-bit ADC result
ADL_DO.H	44H	00	R	ADH_DO[9:2]								

ADH_DO[9:0] (Only read): 10-bit Signed ADC Data Output

*** The decouple capacitor (10uF) must be as near as possible to VCC and VSS.*

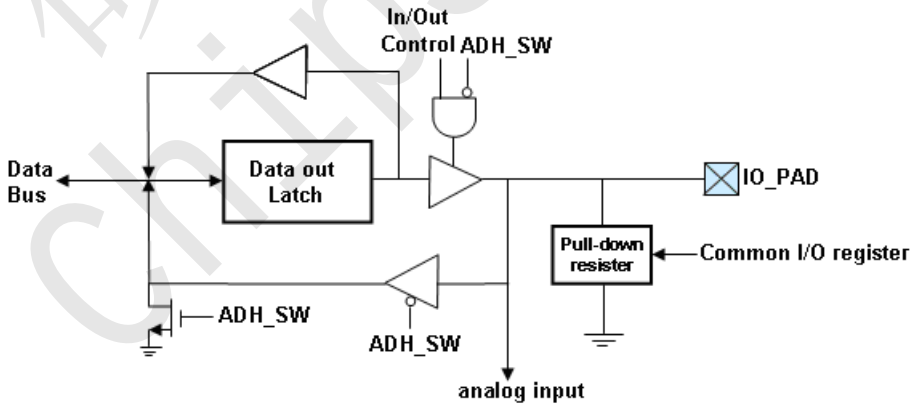

Figure 7.9 ADC External I/O Input PAD Diagram

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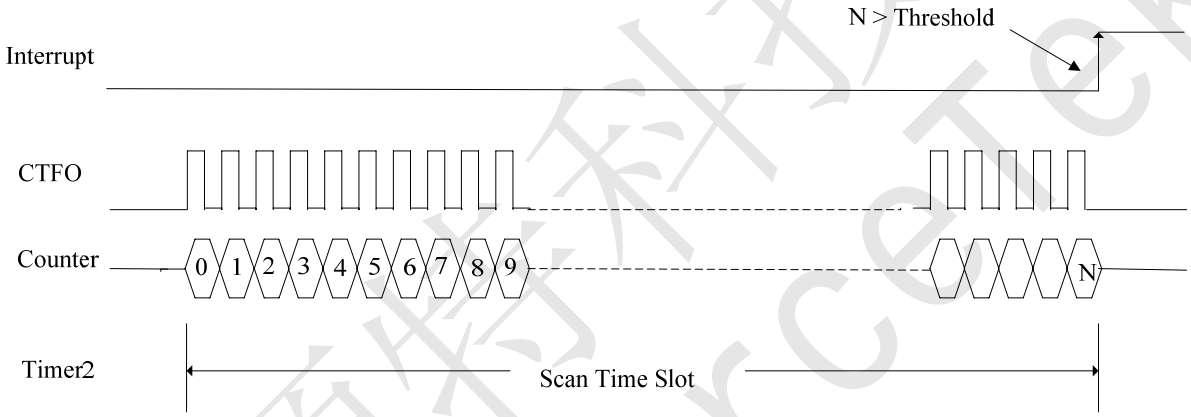
7.7 Anti-noise Touch Controller

The touch controller provides two modes for different case. One mode is low power mode and other is acc mode. Touch controller is equipped with one robust charge-to-frequency circuit, can provide stable sensing under a wide variety of changing conditions.

7.7.1 Features

- The charge-to-frequency circuit doesn't need to use any capacitor.
- Provides two modes for different case.
- Provides an interrupt for efficient programming.

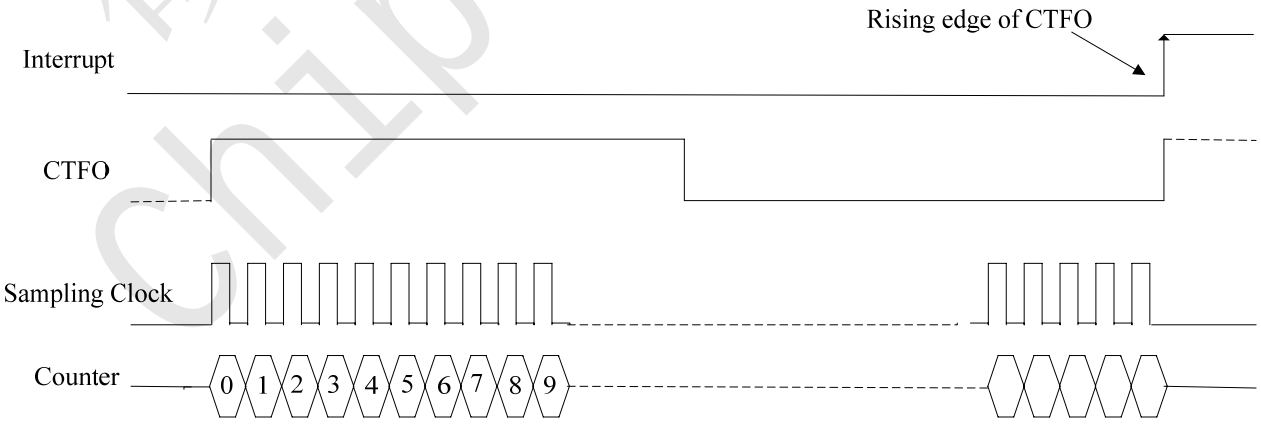
7.7.2 Lower Power Mode



Lower Power Mode is enabled at the period of CPU sleep. And the charge-to-frequency circuit output CTFO signal to counter of touch controller. The counter is counting by CTFO signal at the period of time slot. Scan Time slot can be programmable(See LP_SCAN_TIME).

If counting number N of counter is larger than the specific threshold at the period of time slot, the touch controller will generate an interrupt to CPU and wake up CPU.

7.7.3 ACC Mode



ACC Mode is enabled at the period of CPU running. And the charge-to-frequency circuit output CTFO signal to touch controller. The counter is counting by sampling clock at one CTFO period or several CTFO periods. Sampling clock rate and the number of CTFO several periods can be programmable.

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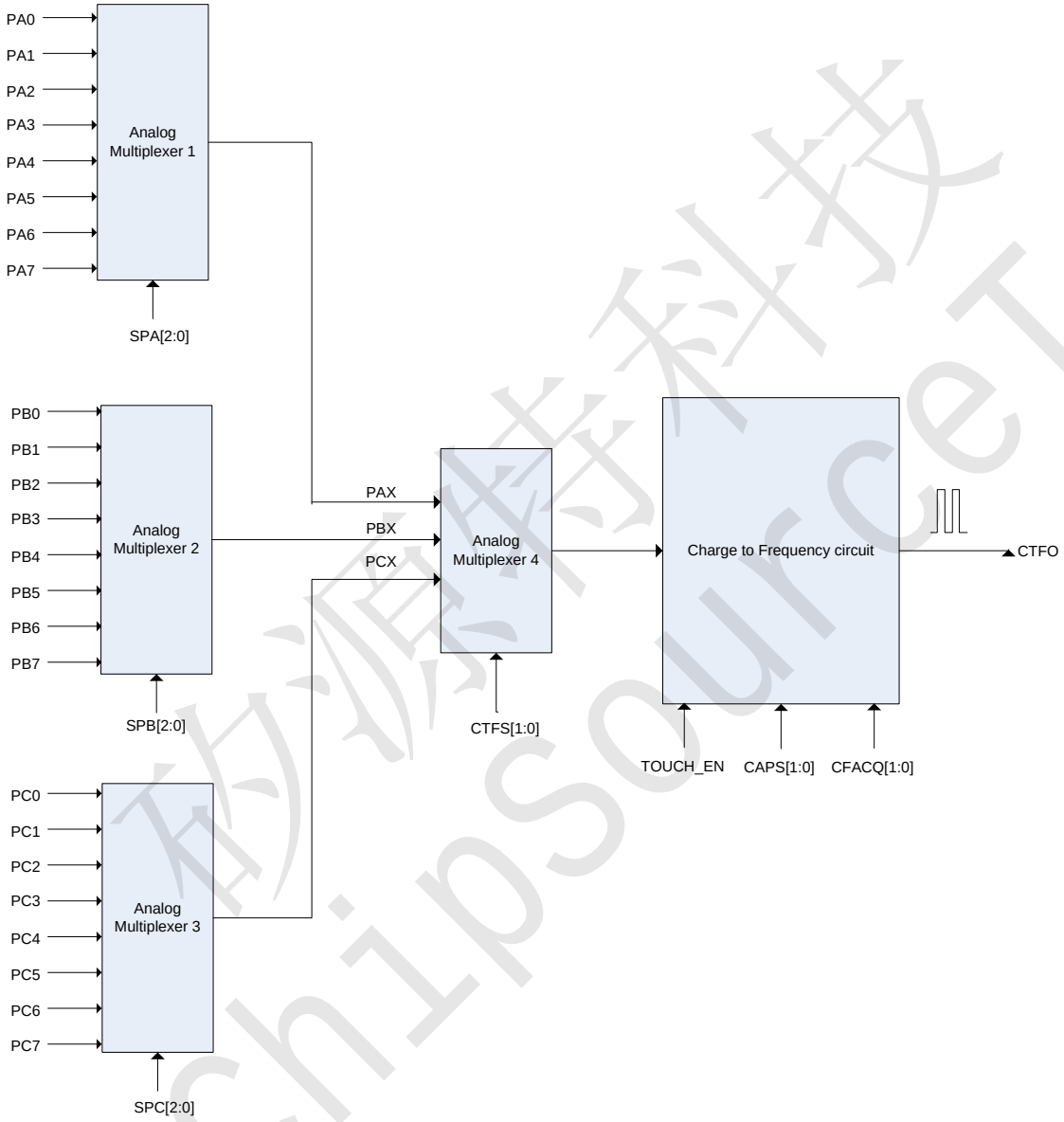
When the counter stops to count after one CTFO period or several CTFO periods, the touch controller will generate an interrupt to CPU.

7.7.4 I/O Pin Select Diagram



SPA[2:0] : 000: PA0, 001:PA1, 010:PA2, 011:PA3, 100: PA4, 101: PA5, 110:PA6, 111:PA7

SPB[2:0] : 000: PB0, 001:PB1, 010:PB2, 011:PB3, 100: PB4, 101: PB5, 110:PB6, 111:PB7

SPC[2:0] : 000: PC0, 001:PC1, 010:PC2, 011:PC3, 100: PC4, 101: PC5, 110:PC6, 111:PC7

CTFS[1:0] : 00: NC, 01:PAX, 10:PBX, 11:PCX

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7.7.5 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
TOUCH_CTL.L	04H	00	W	STR_TIMER	SET_THRESHOLD	SET_CHARACTER	SET_PIN_SEL	SET_LP_SCAN	ACC_MODE	TOUCH_IEN	TOUCH_EN	Control Register Low Byte
TOUCH_CTL.H	04H	00	W	-	-	-	-	-	-	CHG_TOUCH_CNT_CLK	CLR_TIMER	Control Register High Byte
TOUCH_CTL.L	04H	00	R	Touch counter[7:0]								Control Register Low Byte
TOUCH_CTL.H	04H	00	R	TOUCH_INT	0	Touch counter[13:8]						Control Register High Byte

TOUCH_EN: 1-> Touch function enable, 0-> Touch function disable

TOUCH_IEN: 1-> Touch interrupt enable, 0-> Touch interrupt disable

ACC_MODE: 1-> ACC mode, 0-> Low power mode

SET_LP_SCAN: Setting Low power mode registers.

SET_PIN_SEL: Setting SPA, SPB, SPC, CTFS registers.

SET_CHARACTER: Setting character of touch.

SET_THRESHOLD: Setting threshold of touch.

STR_TIMER: Start touch counter at acc mode.

CLR_TIMER: Clear touch counter to 0 at acc mode.

CHG_TOUCH_CNT_CLK: Change clock source of touch counter.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
TOUCH_DAT	05H	00	W	Write_DATA_Buffer[15:0]								Write Data Value
TOUCH_DAT.L	05H	00	R	Touch counter[7:0]								Data Register Low Byte
TOUCH_DAT.H	05H	00	R	TOUCH_INT	LP_WAKEUP	Touch counter[13:8]						Data Register High Byte

Touch_counter[13:0] : Touch Counter

TOUCH_INT : Touch interrupt flag

LP_WAKEUP: Touch wakeup flag at Low Power MODE

OPTION	Write_DATA_Buffer[15:0]															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SET_PIN_SEL =1	-		CTFS		-	SPC			-	SPB			-	SPA		
SET_CHARACTER =1	Acc_loop_number				FREQ_SEL	CTFA			-	-	CAPS		*2	*1	CFACQ	
SET_THRESHOLD =1	-	-	Threshold													
SET_LP_SCAN	-	-	-	*3	LP_SCAN_TIME				LP_STOP_TIME							

SPA[2:0] : Port A selection input pin of touch circuit

SPB[2:0] : Port B selection input pin of touch circuit

SPC[2:0] : Port C selection input pin of touch circuit

CTFS[1:0] : Touch circuit input selection pin

CFACQ[1:0] : Transfer times for save power consumption 00: 1 time, 01: 2 times, 10: 3 times, 11:4 times

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CAPS[1:0] : Select internal capacitor 00: 4PF, 01: 8PF, 10: 12PF, 11:15PF

CTFA[1:0] : Adjust touch circuit basic frequency 00: 400KHz, 01: 500KHz, 10: 600KHz, 11: 350KHz

FREQ_SEL[1:0] : Sampling Clock frequency 00: 65.536MHz, 01: 32.768MHz, 10: 16.384MHz, 11: 8.192MHz

Acc_loop_number [3:0] : The loop number of CTFO period. (Max: 16 CTFO periods)

CTFVFEN(*1): Select VDD for touch circuit power

CFIS(*2) : Change input type for CTF circuit

LP_STOP_TIME: STOP TIME at Low Power MODE

[time = 122.07us x (1+ LP_STOP_TIME), range:8'h0~8'hff]

LP_SCAN_TIME: SCAN TIME at Low Power MODE

[time = 122.07us x LP_SCAN_TIME , range:4'h1~4'hf]

DIS_LP_STOP(*3): Disable STOP TIME at Low Power MODE

Note: Once The Touch Function at IDE OPTION is enable, INT3 enable bit decide whether to start RTC timer. In other word, INT3 bit is enable, then start RTC timer, INT3 bit is disable, then stop RTC timer.

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8. CST16P161A Others

8.1 Spread Spectrum Clocking (SSC)

CST16P161A provide software algorithm with SSC hardware to reduce CHIP EMI. This function can reduce EMI by dynamically adjusting frequency.

Note: Please see Tritan Macro Liberary for reference.

8.2 Low battery detector

Low battery detector is used to detect the "Vlbd" by a 1.2V bandgap reference for VCC derivative. It must set ADH_EN = 1 (ADL_CFG0.H.b15) for enable the sensor reference voltage and set ADH_SW[9] = 1 for ADC input.

** (The accuracy of low battery detector is ± 4% in CST16P161A)

Note: Please see Tritan Macro Liberary for reference.

8.3 Microphone

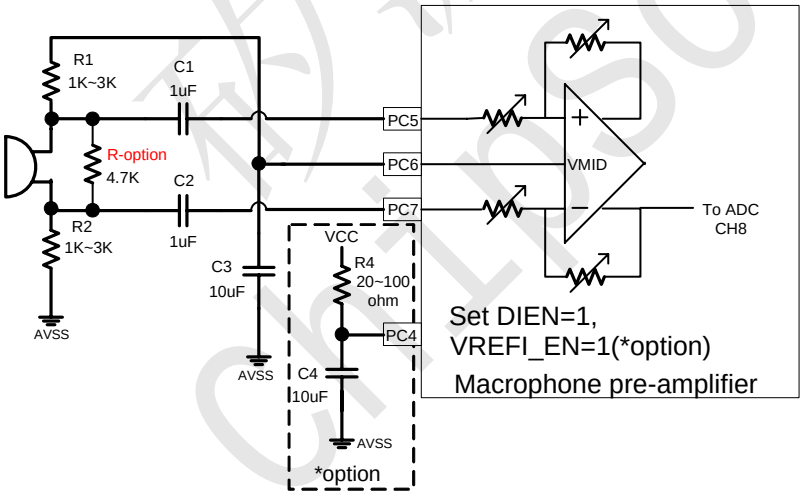
Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
MIC.L	64H	30	R/W	-	-	**PGA[5:0]**						Microphone & Temperature Sensor
MIC.H	64H	00	R/W	**LOPEN**	-	**SLOP**		-	-	**DIEN**	**MIC_EN**	

***MIC_EN:** Microphone Enable

***DIEN:** Microphone differential input Enable

***PGA[5:0]:** Microphone Amplifier Gain

* **VREFI_EN:** ADC VREF input (PC4) enable bit (ADL_CFG0.H.b13, Address : 40H)



*option:

If the external SPI flash is used, suggest use this option for noise reduction. (When VREFI_EN is set, R4 and C4 must be connected)

R-option: It can help to adjust PC6 bias voltage, if microphone impedance (Rmic) is to high (When Rmic > 8K)

Fig 8.4.1 Microphone differential input application circuit

** R1 and R2 must be adjusted to PC6 bias voltage near (1/2 VCC - 0.1V) for different microphone impedance. (VCC = the highest operating voltage)

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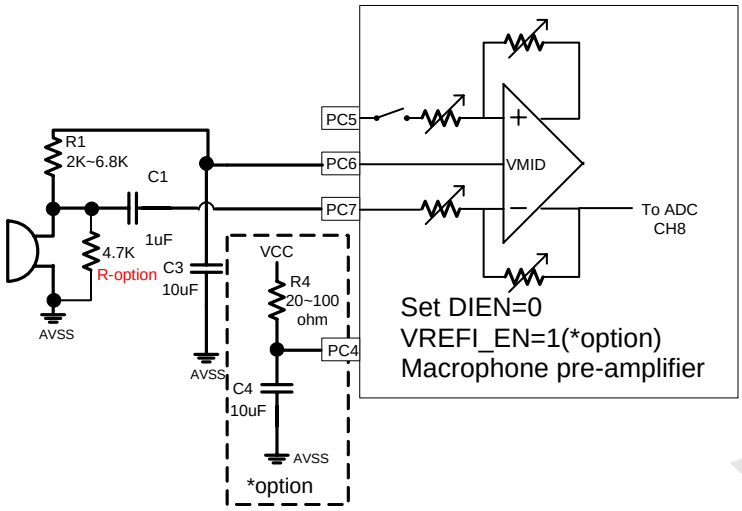

*option:
If the external SPI flash is used, suggest use this option for noise reduction.
(When VREFI_EN is set, R4 and C4 must be connected)
*R-option: It can help to adjust PC6 bias voltage, if microphone impedance (Rmic) is to high (When Rmic > 8K)

Fig 8.4.2 Microphone single end input application circuit

** R1 must be adjusted to PC6 bias voltage near (1/2 VCC - 0.1V) for different microphone impedance. (VCC = the highest operating voltage)

There is a programmable gain amplifier (PGA) in the CST16P161A for microphone pre- amplifier. Default gain of the single end input mode is 34db, (PGA [5:0] = 20h).Each gain step is 1db. Maximum gain is 52db (PGA [5:0] = 2Fh), minimum gain is 2db in single end input mode. The default gain of the differential input mode is 40db. Maximum gain is 70db (PGA [5:0] = 3Bh), minimum gain is 8db in differential input mode. PGA Input resistance is ~ 2Kohm.PGA output is connected to ADC input (ADH_SW [8]).

The table of the gain programmable range

PGA [5:0]	Single end input (db)	Differential input (db)
000000	2	8
000001	6	12
000010	7	13
000011	8	14
Each step 1db	9 ~ 33	15 ~ 39
100000 (default gain)	34	40
Each step 1db	35~50	41~56
101110	51	57
101111 (2F)	52 (Maximum gain)	58
Each step 1db in Differential input	na	59 ~ 68
111010	na	69
111011 (3B~3F)	na	70 (Maximum gain)

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9. CST16P161A System Control

9.1 Halt Mode & Wake up

The CST16P161A is changed into HALT mode (system clock stop, RTC stop by Option setup) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The RTC timer, PA0~PA7 and PB0~PB7 are supporting the wake-up MCU function when related I/O port raising/falling edge which selects by option. The program counter will be 04H when HALT instruction executed immediately; in addition, MCU will release HALT state and program counter go-to next address after 16us stable clock(system clock) when wake up condition occurred. During the Halt mode period, the SRAM will keep their previous data without changing, yet INTENA register will auto clearly.

Note: The CST16P161A provide a new wake up mode, user can enable this mode by setting enable bit at IDE OPTION. If new wake up mode is enable and wake up CPU by interrupt, the program counter will go to interrupt service routing first, and then go to 04H wake up address.

9.2 Watch Dog Timer Reset (WDT)

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
ClrWDT	1DH	XX	W									Clear WDT
RealT	1DH	0000	R	RealT[15:0]								Watch Dog Real-Time Counter

The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence of instructions caused by accident condition, avoiding dead lock of MCU program. Software shall run an "clear watch dog timer"(CLRWDT) instruction before this timer time out. It will generate a reset signal to reset whole system when WDT overflow.

WDT will be reset when wake-up from halt or after power on or software clear. In test mode, watch dog timer will be disabled no matter watch-dog-timer is time-out or not. If programmer read the "RealT" register, it can get the content of watch dog timer base on 31.25us.

The reset watch dog timer code syntax is strongly recommended as: "**CLRWDT = AR**".

9.3 Low Voltage Reset

When VDD power is applied to the chip, the low voltage reset is initially enabled by default, it will be disabled when in halt mode. The internal system reset will be generated if VDD power below about 2.2v.

The normal operation of LVR is always enable expect disable in HALT mode.

9.4 Reset System

The CST16P161A reset is come from four signals which are power on reset, low voltage reset(LVR), external "RSTBIN" pin and WDT overflow reset. A dedicated resetb input pin is provided to reset this chip. For normal operation of this chip, a good reset is needed. This pin has 50K ohm pull up resistor. The operation frequency of MCU will go back to OTP page mode when reset occurred.

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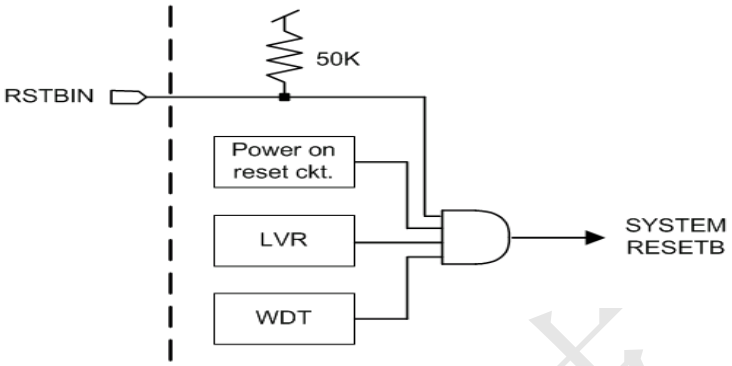

Figure 9.1 Reset system block diagram

9.5 Clock System Architecture

The CST16P161A clcok system supports internal ROSC(65.536MHz) for System Clock, and External Crystal 32768Hz or Low power RC oscillator(32768Hz ± 2%) for RTC function.These crystal pins X32KI and X32KO can be shared with PortC[0], and PortC[1] respectively.

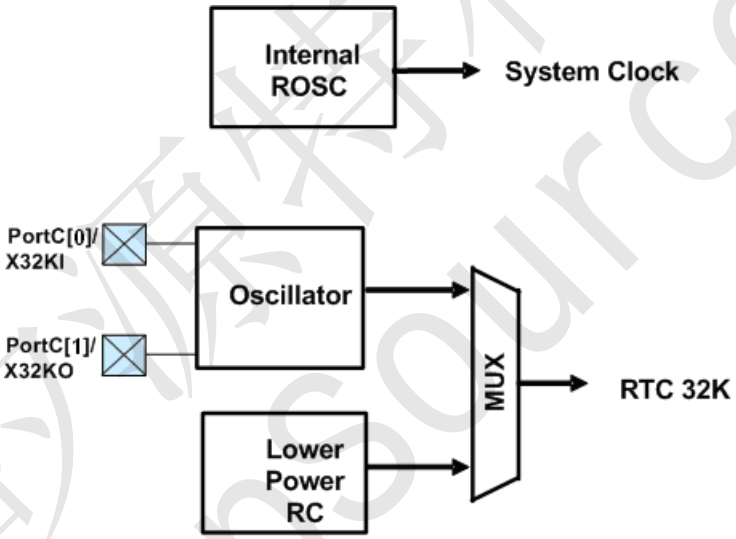

Figure 9.2 Clock System Configuration

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10. CST16P161A Electrical Characteristics

10.1 Absolute Maximum Rating

Parameters	Symbol	Value	Unit
DC Supply Voltage	VDD	<5.5	V
Input Voltage	Vin	-0.5 to VDD+0.5	V
Operating Temperature Range	Ta	0 to 75	℃
Storage Temperature Range	Tstg	-50 to 150	℃

10.2 DC/AC Characteristics

VDD=3.0V, Ta=25℃ unless otherwise noted

Parameters	Symbol	Minimum	Typical	Maximum	Test Condition
Operating range	VDD	2.4 V	-	5.5 V	
RC oscillator frequency	Frc1		10.92MHz ±1%		
Low power RC oscillator frequency	Frc2		32768Hz ±2%		
Halt Current	Ihalt1		<3uA	5uA	All function off
VPPX pin programming voltage	VPPX		7.5 ±0.25V		
Operating Current	Iop		10mA		no load
input high voltage	Vih	0.8 VDD			
input low voltage	Vil			0.2 VDD	
input leakage Current	Ilk			0.1 uA	
output high voltage	Voh	0.95 VDD			no load
output low voltage	Vol			0.05 V	no load
output high current1	Ioh		12 mA		Vout=2.4V, PortA[7:0] ,PortC[7:0]
output high current2	Ioh		12 mA		Vout=2.4V, PortB[7:0]
output low current1	Iol		-20 mA		Vout=0.8V PortA[7:0],PortC[7:0]
output low current2	Iol		-25 mA		Vout=0.8V PortB[7:0]
pull-down resistance	Rpd		50 K ohm		pins with pull-down, Port A,B,C,

10.3 10bit ADC Characteristics

(Ta = 25℃, VCC = 2.4 ~ 5.5V, unless otherwise noted)

Parameters	Symbol	Minimum	Typical	Maximum	Unit
ADC clock frequency	FADC			1	Mhz
Sample rate	Fsample			71.2	Khz
Differential Nonlinearity	DNL		±1		LSB
Integral Nonlinearity	INL		±1		LSB
Offset error	OS		±1		LSB
No Missing Code	NMC		9		Bit
Input capacitance	INC		2		pF
Input resistance	INR			100 *1	K

*1. Input resistance must small than 100K for FADC=4Mhz and TAD=2*FADC.

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11. CST16P161A Development Support

CST16P161A™ family series are supported with full range of hardware and software development tools:

- Integrated Development Environment (IDE)
  - CST16DevIDE software
- CST16DevIDE contains
  - TxPASM Assembler
  - TxPCC C Compiler
  - TxPLink Object Linker
  - TxPLib Library Management
- Simulator
  - CST16SIM software Simulator
- Emulator
  - CST16ICE circuit hardware Emulator
  - **Emulator doesn't support PWM Mute function for emulation, user need to notice this difference between Emulator and Real Chip**.

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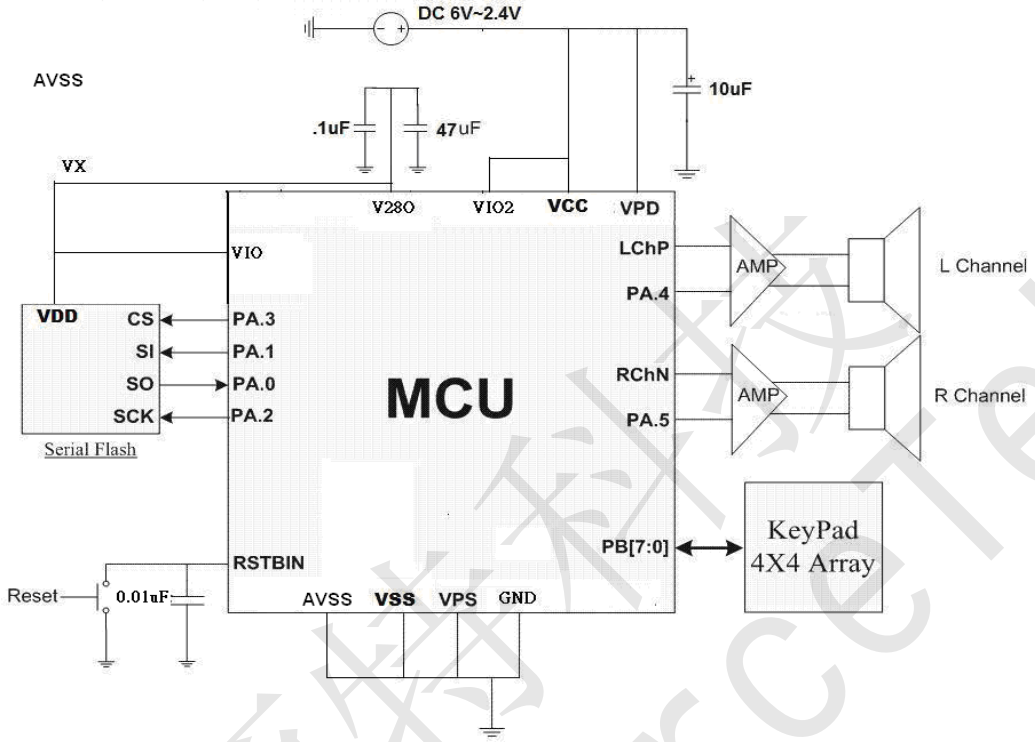
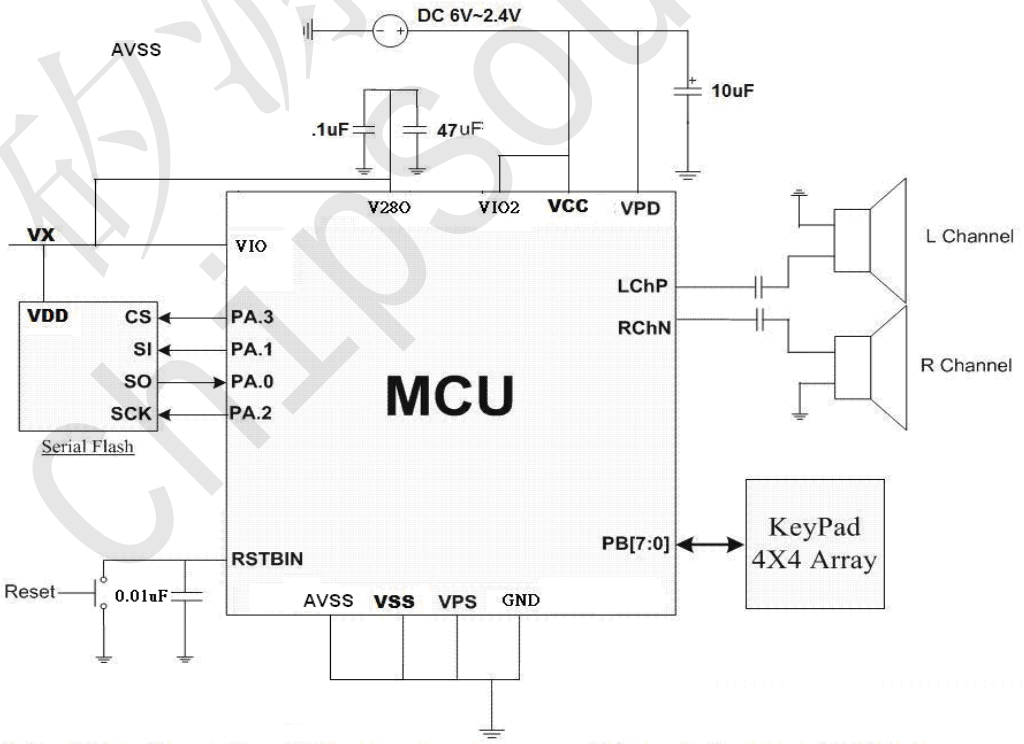
12. CST16P161A Application Circuit:

Application Circuit 1.a : Stereo 16-bit PWM AMP output with Serial Flash



Notice: VX could come from LDO or other power source, which meets the spec. of SPI Flash.

Application Circuit 1.b : Stereo 15-bit PWM output with Serial Flash



Notice: VX could come from LDO or other power source, which meets the spec. of SPI Flash.

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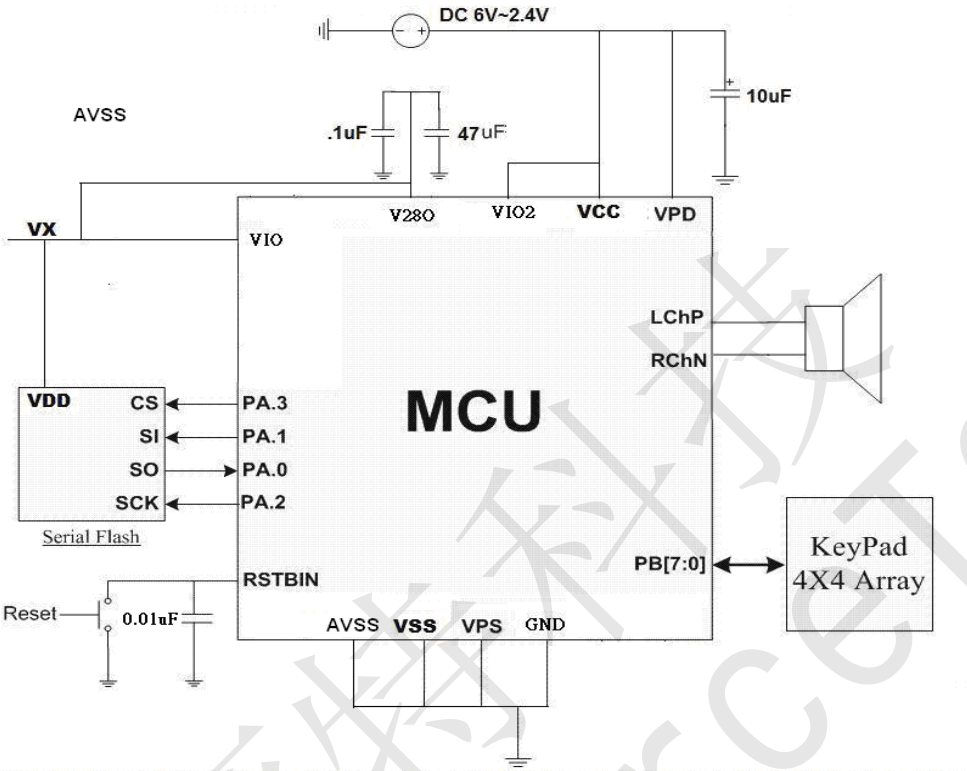
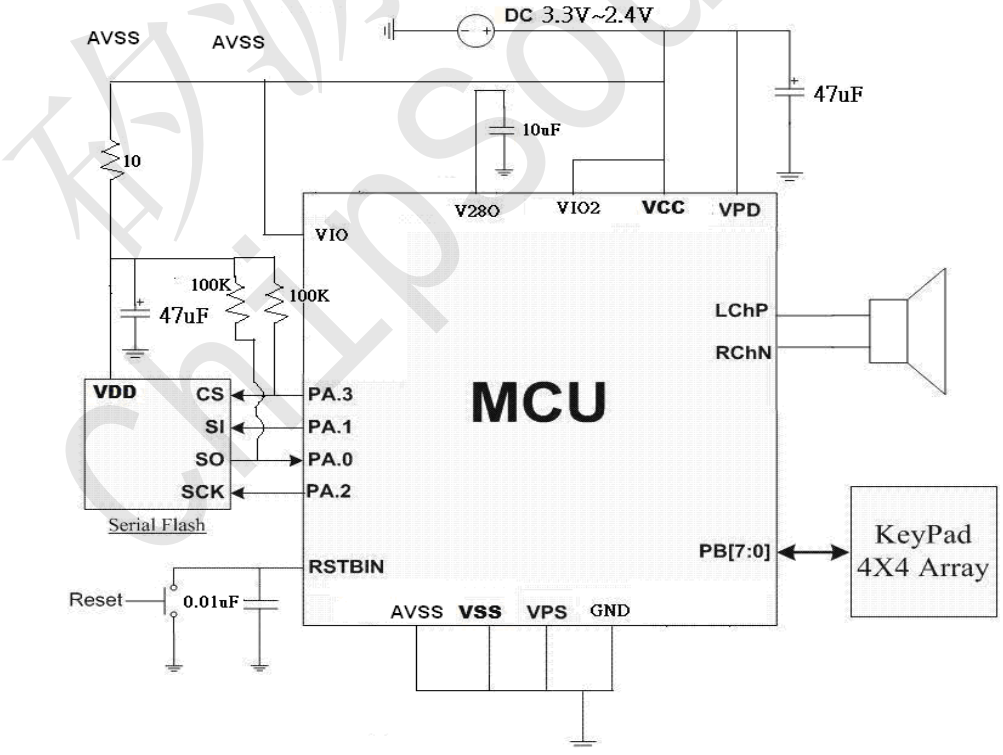
Application Circuit 1.c : Mono16-bit PWM output with Serial Flash (1.5V Battery x 4)



Notice: VX could come from LDO or other power source, which meets the spec. of SPI Flash and SD Card.

Application Circuit 1.d : Mono16-bit PWM output with Serial Flash (1.5V Battery x 2)



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13. CST16P161A Appendix:

A1 SPI Operation Sequence

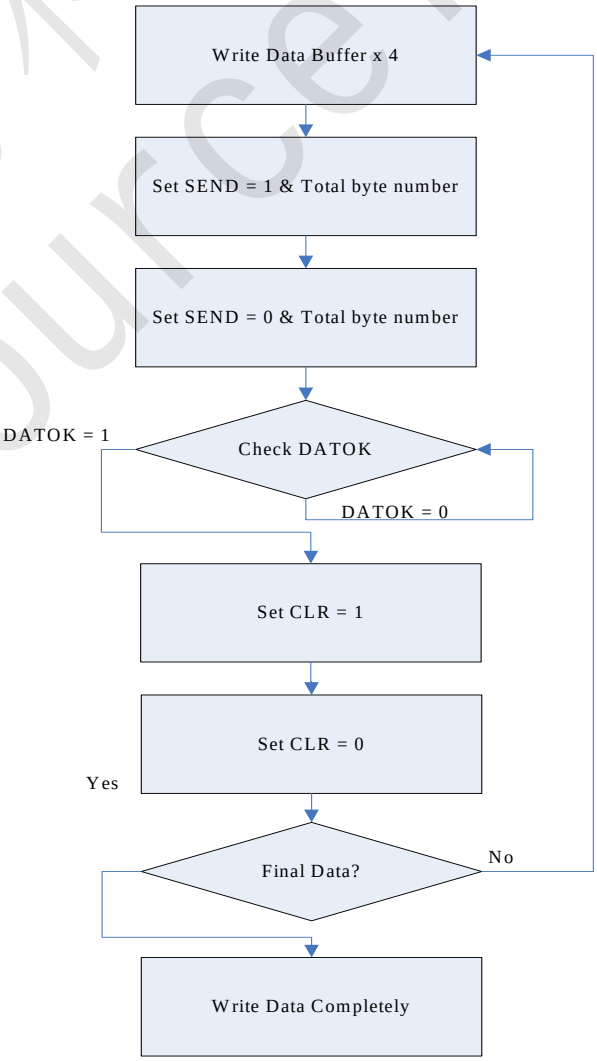
A1.0 Initial Process

```
set io[IOC_PA].b3          // set output port
set io[STATUS].b8          // Enable SPI Control
set io[PortA].b3           // CS=1
set io[SPI_CTRL].b11       // set ICS = 1
```

A1.1 Sending Data Process

```
clr io[PortA].b3                // CS =0
clr io[SPI_CTRL].b11            // ICS=0
// page write 256 bytes
cx = 0x1f;
i0      = Data_Buf.n0
i0.h    = Data_Buf.n1
SPI_write_data_loop:
io[SPI_DATA] = rm[i0++];
io[SPI_DATA] = rm[i0++];
io[SPI_DATA] = rm[i0++];
io[SPI_DATA] = rm[i0++];
push ar;
// set total byte number & send data
ar = 0x18;
ah = 0x00;                      // speed
io[SPI_CTRL] = ar;              //set SEND = 1;
clr io[SPI_CTRL].b4             // set SEND = 0;
call   Check_Tran_OK
loop   SPI_write_data_loop
set io[PortA].b3                // CS =1
set io[SPI_CTRL].b11            // ICS=1

Check_Tran_OK:
test io[SPI_CTRL].b7
if eq jmp Check_Tran_OK
set io[SPI_CTRL].b6             // CLR = 1
clr io[SPI_CTRL].b6             // CLR = 0
Check_Tran_OK_End:
rets
```



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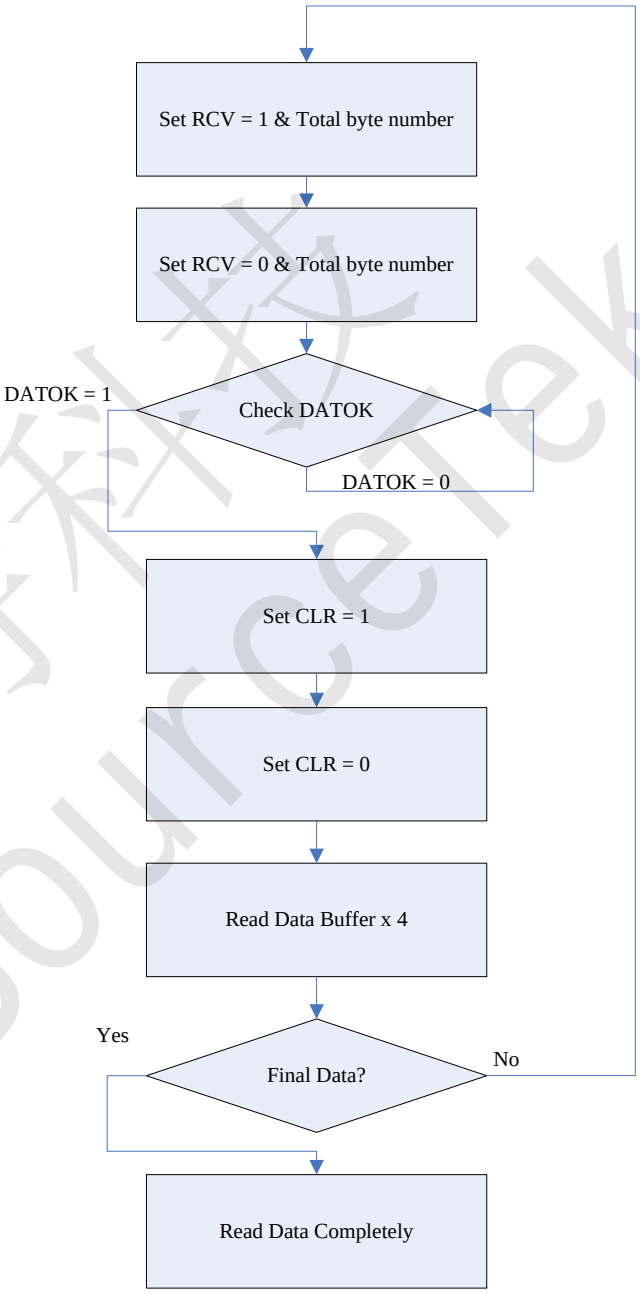
A1.2 Receiving Data Process

```
            clr io[PortA].b3                // CS =0
             clr io[SPI_CTRL].b11           // ICS=0


             i0      = Data_Buf.n0
             i0.h    = Data_Buf.n1
            // receive data(256 bytes)
            cx = 0x1f;
SPI_read_data_loop:
             ar = 0x28;
             ah = 0x00;                     // speed
             io[SPI_CTRL] = ar;             // Set RCV = 1;
             clr io[SPI_CTRL].b5            // Set RCV = 0;
            call    Check_Tran_OK
            rm[i0++] = io[SPI_DATA];
             rm[i0++] = io[SPI_DATA];
             rm[i0++] = io[SPI_DATA];
             rm[i0++] = io[SPI_DATA];
            loop    SPI_read_data_loop
             set io[PortA].b3               // CS =1
             set io[SPI_CTRL].b11           // ICS=1



Check_Tran_OK:
             test io[SPI_CTRL].b7
             if eq jmp Check_Tran_OK
             set io[SPI_CTRL].b6    // CLR = 1
             clr io[SPI_CTRL].b6    // CLR = 0
Check_Tran_OK_End:
            rets
```



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14. CST16P161A Revision history

REVISION	DESCRIPTION	PAGE	DATE
V1.0	New establish		2014/6/19
V1.1	Modify Microphone Circuit	38, 39	2014/12/9
V1.2	Modify ADC clock	31	2015/2/24
	Modify output high current2 / output low current2	42	2015/2/24
V1.3	Modify Microphone Circuit	38, 39	2015/3/25
	Remove temp. sensor		2015/3/25

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